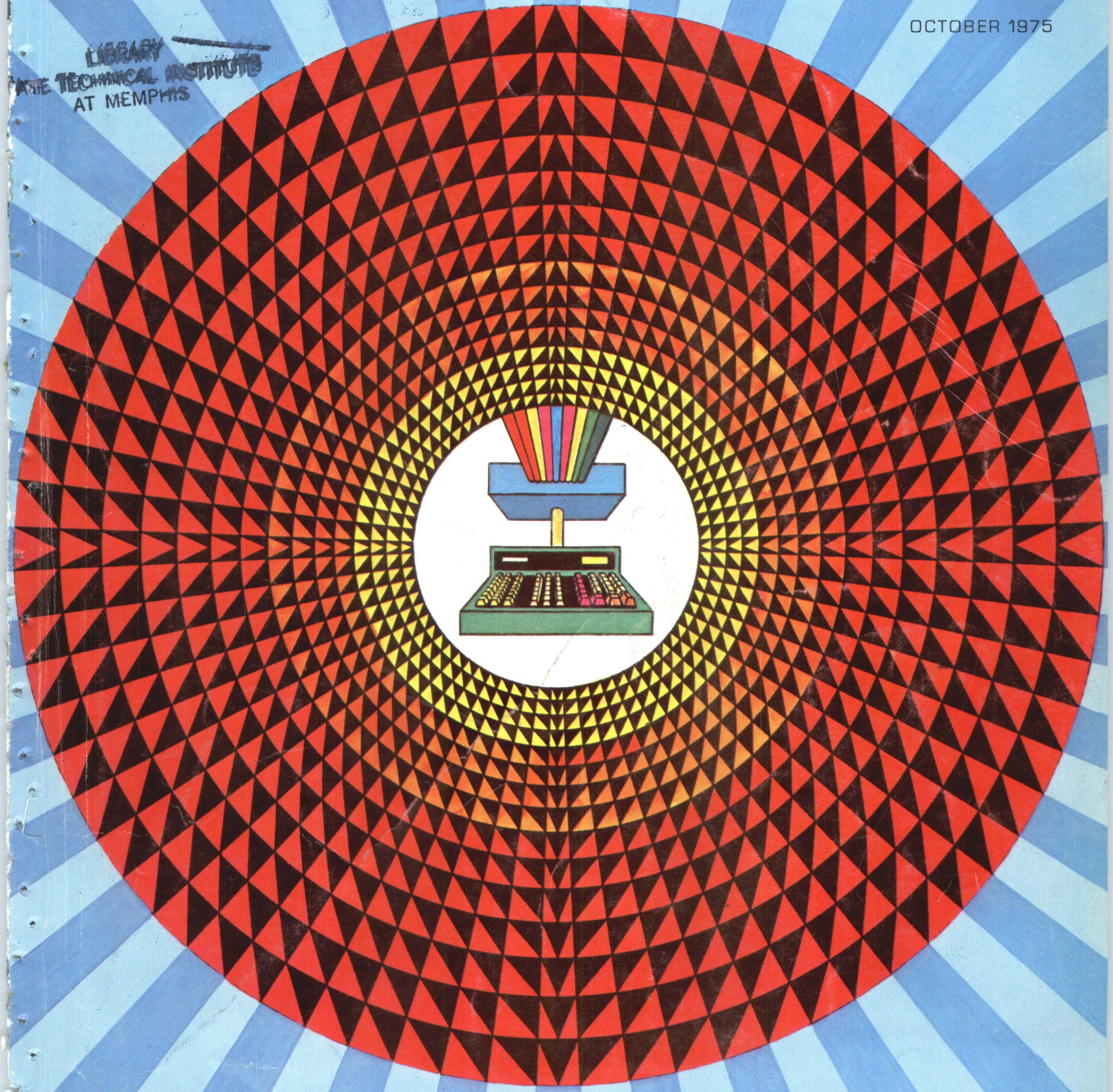
COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

OCTOBER 1975



PROGRAMMABLE CALCULATORS CONTROL DATA ACQUISITION SYSTEMS

USING A MICROPROCESSOR: A REAL-LIFE APPLICATION PART 2—SOFTWARE

OCR SYSTEM DESIGN BENEFITS FROM TECHNOLOGICAL ADVANCES

Tally's printer line is going places...

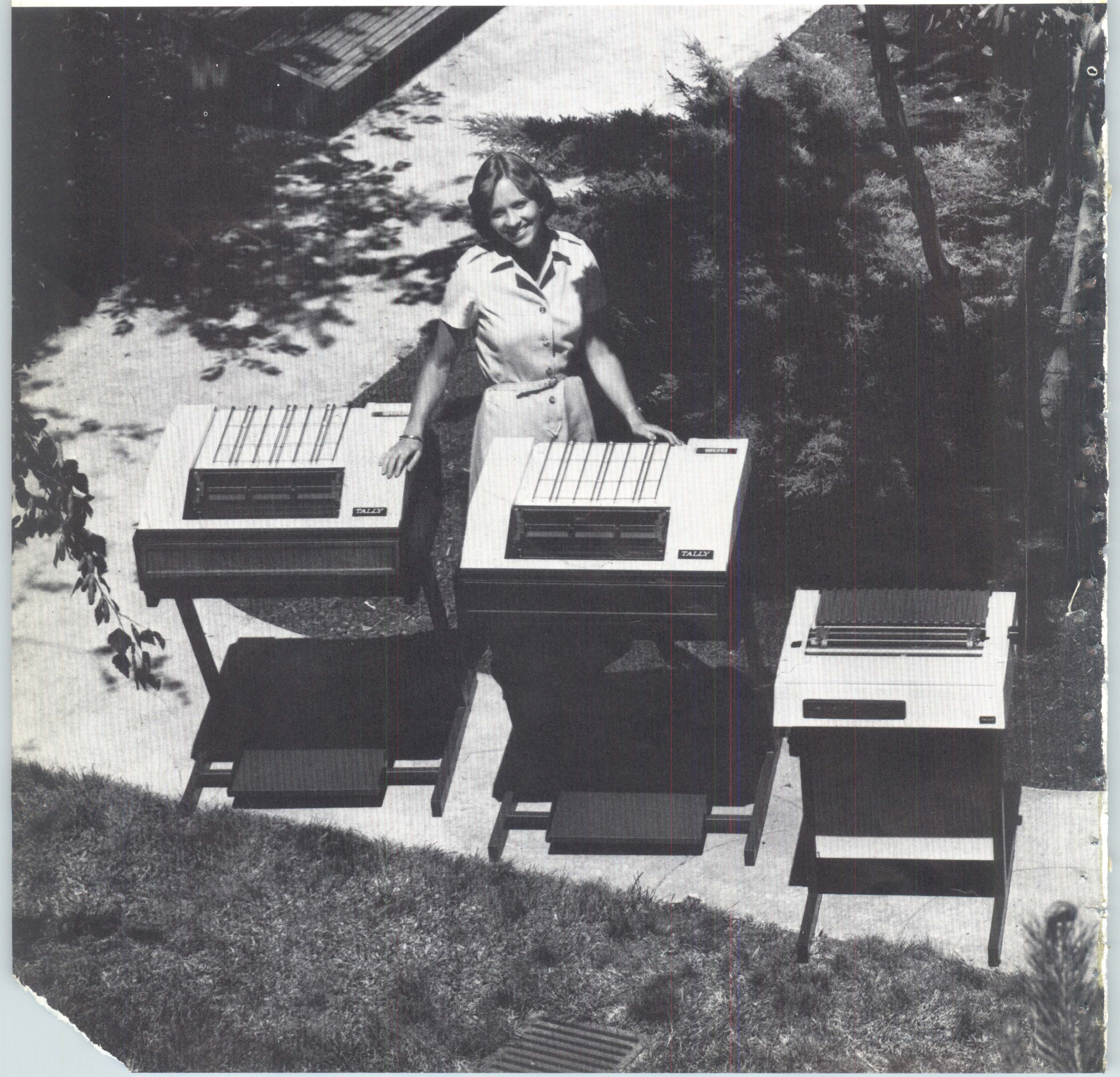
Tally's renowned 200 line per minute line printer for the long run is now backed up with 125, 300 and 400 lpm. There's more. The beginning of a line of serial printers. The Series 1000. First off the blocks is a 120 character per second, 132 column, high reliability data processing machine.

Now, with this fine family of printers, you can pick the

Model 2100
125 lines per minute
132 columns
7 x 8 comb matrix print
Multi-part forms to 14⅞"
Up to 8-channel VFU
Many parallel interfaces
1200 Baud communications

Model 2200
200 lines per minute
132 columns
5 x 7 comb matrix print
Multi-part forms to 14⅞"
Up to 8-channel VFU
Printer emulating interfaces
Mini controllers

Model 1120
120 characters per second
132 columns
9 x 7 high fidelity print
Multi-part forms to 15"
2-channel VFU
Many parallel interfaces
Asynchronous communications



up to 400 lines per minute...down to 120 characters per second.

price/performance package that best suits your system. And be comfortable in knowing that Tally reliability won't let your customer down in the middle of a print run.

Talk to Tally today about these low cost, high performance printers. You'll enhance the value of your total system package. Tally Corporation, 8301 South 180th Street, Kent, Washington 98031. Phone (206) 251-5645.

Model 4300
300 lines per minute
132 columns
9 x 9 comb matrix print
Multi-part forms to 19"
Up to 12-channel VFU
20 ips slew
Interfaces and controllers

Model 4400
400 lines per minute
132 columns
9 x 7 comb matrix print
Multi-part forms to 19"
Up to 12-channel VFU
20 ips slew
Interfaces and controllers

CIRCLE 1 ON INQUIRY CARD

TALLY
has something new

If you punch cards, read cards or do anything else with cards,

we want to talk to you.

We want to talk to you about the Tab 501 Data Entry Microprocessor.

About the unique versatility and operating capabilities resulting from its built-in microprocessor, RS-232C interface and unmatched performance characteristics:

- Minicomputer card input or output.
- Data transmission via modem or cable for terminal applications.
- Interfacing to virtually any type of data entry or processing system.
- On-line or off-line versatility.
- Reading, punching, printing, verifying and interpreting capabilities.
- Attractive purchase or lease plans.

We want to tell you about our standard features.

- Constants from memory—up to 220 columns.
- Up to 28 program levels with automatic sequencing.
- Instant verification.
- Completely automatic error correction.
- High speed character duplication.
- Exceptionally quiet.
- Unparalleled operator acceptance of over 2,000 installed units.
- Easy to learn—easy to operate.

Let's talk about "specials." We want your specials. Special applications. Special operating characteristics. Special interfaces. Special keyboard requirements. Because the Tab 501 Data Entry Microprocessor has this unique flexibility, we can give you what you want—easily and inexpensively. It's worth talking about.

Gentlemen: Let's talk.

Name__________

Company__________

Address__________

City______ State______ Zip______

Telephone__________

Let's talk:

☐ Interfaces. ☐ Special requirements.

☐ Terminal applications. ☐ Send more information.

TAB
PRODUCTS CO

2690 Hanover Street
Palo Alto, California 94304

CIRCLE 2 ON INQUIRY CARD

THE MAGAZINE OF DIGITAL ELECTRONICS

COMPUTER DESIGN

OCTOBER 1975 • VOLUME 14 • NUMBER 10

FEATURES

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BPA CIRCULATION OVER 55,000

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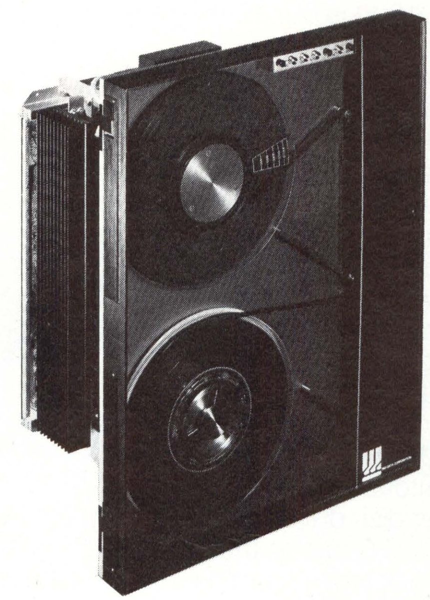
SIMPLICITY

(sim plis′i tē) n., the state of being simple, uncomplicated and straightforward.



At Digi-Data, simplicity is a magnetic tape transport built on a machined aluminum plate with direct drive motors, low inertia arms, superb maintenance accessibility, and no plastic cosmetics. This clean and straightforward design is the result of over a decade of concentration in tape-handling technology.

To the End-user, simplicity is a single supplier who manufactures mag tape transports, formatters, and software-compatible computer interfaces.

For the OEM, simplicity generates higher profit margins without a sacrifice in performance or reliability— margins that result from low acquisition costs and minimal maintenance.

Simplicity permits a lower cost to manufacture—a savings that is passed directly through to you.

Simplicity promotes high reliability with a low MTTR—eliminating the need for an excessive spares inventory and requiring fewer service calls for your CE's. Digi-Data protects your reputation for reliability and enhances your image among customers and prospects.

Quantity one price of a 45 ips NRZI transport is
$2,975.

Complete minicomputer mag tape systems from
$4,750.

Substantial OEM discounts available.

DIGI-DATA CORPORATION ®

Supplier of magnetic tape transports and systems.

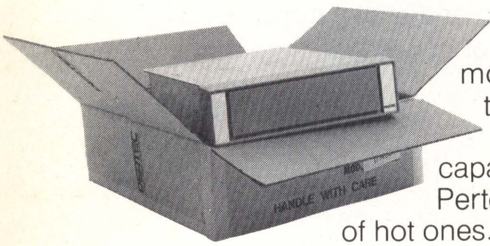
8580 Dorsey Run Road, Jessup, Maryland 20794 (301) 498-0200

Digi-Data Europe

Flüestrasse 632 5313 Klingnau, Switzerland Tel. 056 45 3610

Try our co layaway

Hurry.
To the disk drive sale of the year.
Featuring year-end clearance prices.
On the fastest selling, low-cost, fixed-media moving head disk drives in the industry.
On brand-new, never-before-advertised units from Pertec.



Orders for two models are greater than current production capacity. So, hurry: Pertec's got a couple of hot ones.

The D1400: Lay it away now.

The new D1400 is our 6 megabyte capacity model.

It offers a combination of outstanding features at exceptionally low cost, including: A 2316-type non-removable platter; bit density of 2200 BPI; track density of 200 TPI; available at either 1500 rpm or 2400 rpm.

Its Pertec-standard interface is compatible with almost every disk drive. And, its chassis (standard 19 inch panel width, by 22.4 inch rack depth, by 5.25 inch height) makes it fit where you want it to fit.

OEM's can use its average seek time of 70 ms and track-to-track seek time of 12 ms to improve the performance of their system design.

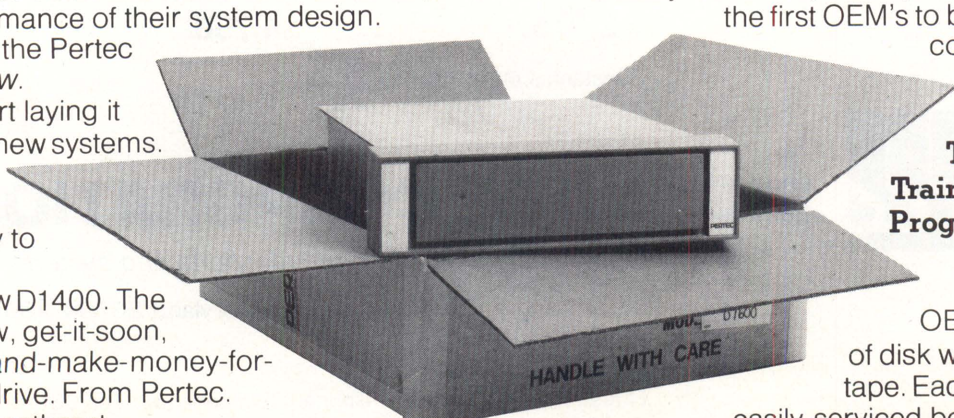
So, buy the Pertec D1400 *now*.

And start laying it into your new systems.

While you smile all the way to the bank.

The new D1400. The buy-it-now, get-it-soon, lay-back-and-make-money-for-you disk drive. From Pertec.

It's a sweetheart.

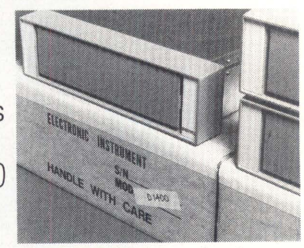


The D1600: Lay it away in December.

The new D1600 is our 12 megabyte capacity model.

(Double the capacity of the D1400: Only 15% more cost than the D1400.)

It offers OEM's a configuration of features that 12 megabyte customers require, including: A 3336-type non-removable platter; bit density of 4400 BPI; track density of 200 TPI; available at either 1500 rpm or 2400 rpm.



Buy at least one of each.

(All the standard features in our 6 megabyte model are standard in the D1600.)

OEM's can specify a Pertec-standard interface or configurations compatible with other disk drives of other manufacturers.

Chassis size? Same as the D1400.

Average seek times? Same as the D1400.

Media protection assuring highly reliable operation and data integrity, improved air filtration and sectoring configurations up to 64 sectors, make the D1600 an OEM favorite.

But there's a catch: You can buy the Pertec high-capacity, low-cost D1600 *now*.

But you can't lay it into your new systems until December.

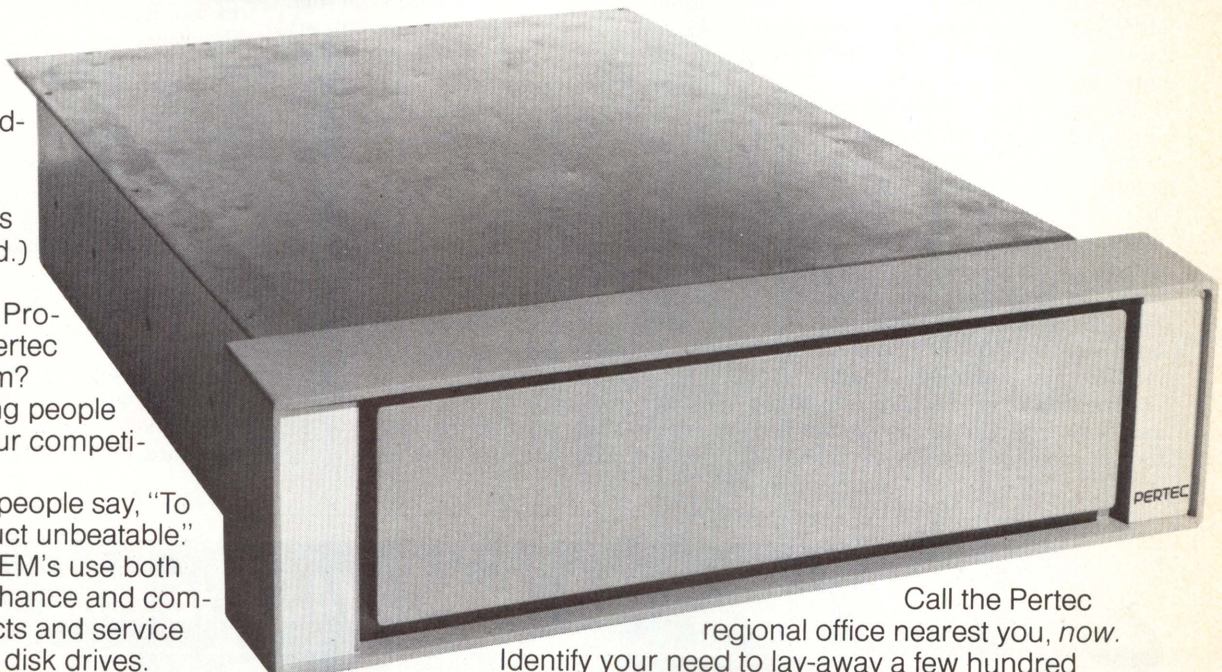
Orders for the D1600 are being accepted now.

So buy it *now*. Lay it away *now*. And be among the first OEM's to be ahead of your competition in December.

The Pertec Training and Spares Programs: Too Much?

The D1400 and D1600 provide OEM's the benefits of disk with the low cost of tape. Each drive has four easily-serviced boards which lift or

nvenient plan.



hinge for immediate access to circuitry. (No other disk drives are so designed.)

Why then a Pertec Training Program? And a Pertec Spares Program?

Our marketing people say, "To drive our competition crazy."

Our product people say, "To make the product unbeatable."

Either way, OEM's use both programs to enhance and complete the products and service behind Pertec's disk drives.

Is too much service too much? Ask Pertec customers, and decide for yourself.

Finally. The Layaway of Layaways: The D1200.

You're looking at Pertec's prototype model D1200, with a 3 megabyte capacity. For the OEM looking for *lower*-capacity, *lower*-cost drives. (After all, why buy a 6 or 12 megabyte capacity when you only need a 3?)

"Will it look like the D1400 and D1600 models?" you ask.

"Will it perform with Pertec reliability?" you probe.

When the D1200 is in volume production, it will *look* like the D1400 and D1600.

And, with the first OEM delivery, it will perform with Pertec reliability.

So, look into the D1200 *now.*

Call the Pertec regional office nearest you, *now.* Identify your need to lay-away a few hundred D1200's for spring delivery.

Then lie back and ask yourself, "Will Pertec really deliver a 3 megabyte disk drive?..."

"Should I wait 'til all my competitors have them?"..."Should I order a D1400 or D1600 now?"..."Or should I order some of each?"

The new Pertec disk drives. Delivering 6, 12 (and shortly, 3) megabyte capacity at OEM low-cost.

Will Pertec deliver?

Not unless you order, *now.*

So, hurry. And lay-away the finest performing fixed-disk drives in the industry.

PERTEC

Call the Pertec regional office nearest you:
Boston (617) 890-6230;
Chicago (312) 696-2460;
Los Angeles (213) 996-1333;
London (Reading) 582-115.
Or write: Pertec,
Peripheral Equipment Division,
9600 Irondale Avenue,
Chatsworth, California 91311.

CIRCLE 6 ON INQUIRY CARD

LETTERS TO THE EDITOR

To the Editor:

In reference to the article by Sidney Davis on digital stepping motors in the May issue, . . . although it is our opinion that the article stated the situation regarding both the PM and VR steppers quite well, we feel somewhat 'left out' since no mention was made of our unique and patented line of steppers which utilize the nutating drive principle.

The use of the nutating principle permits Mesur-Matic to offer stepping motors with extremely fine step angles, for instance, 0.225 or 0.1125 deg at speeds of 5 to 10,000 steps/s. Most VR and PM steppers refer to torque in inch-ounces, whereas the NuSyn is rated in pound-inches with zero backlash, providing for true open-loop operation with no feedback required for positional accuracy.

In addition to the fine step angle and very high torque for motor size, further benefits are in low internal inertia, freedom from resonance problems, and very high acceleration.

To obtain the same, or even similar, fine step angle with either the PM or VR type of stepper requires the use of a gear train with the attendant problems of wrap-up, accuracy, and maintenance mentioned in the article.

Torque available from our NuSyn ranges from 2 to 100 lb-in. in our largest motor, with low internal inertia. Thus the ability to accelerate from 'dead stop' to 6000 steps/s (0.225-deg steps) within 10 ms, with start/stop rates as high as 2500 steps/s.

The NuSyn does not have the resonance problems referred to in the article since it has the ability to momentarily 'lead' or 'lag' the magnetic field without losing control. Internal damping is quite high, which leads to naturally short 'ringing' times.

Philip F. Dolan
Mesur-Matic Electronics Corp
Salem, Mass

To the Editor:

"A BCD Conversion Technique for Teletypewriter Applications" by Ellsworth & Malloch was to me a very interesting article. I read it probably more times and more carefully than any other article you have published since I first started reading your magazine. I think the criticism of the article by J. A. Titus [May 1975, p 6] is about six yards wide of the mark. Everybody knows that UARTs have been "available" since 1971. The last UART I purchased had to be ordered from the factory by the Seattle distributer and took over eight months to get here. Any of the ICs used in the Ellsworth-Malloch circuit can be purchased over the counter in Seattle on a Saturday afternoon.

Jack D. Dennon
Dennon Electronics
Renton, Wash

Letters to the Editor should be addressed:

Editor, Computer Design
Professional Building
221 Baker Avenue
Concord, MA 01742

At last– low prices on Interdata memories.

Plessey Microsystems, the leading independent supplier of minicomputer add-ons, can expand your Interdata memory without putting the bite on your budget; with the PM-716 plug-in memory card.

The PM-716 is offered in 8k and 16k capacity and is fully compatible with all Interdata minicomputers. It is available off-the-shelf for much, much less than the Interdata equivalent.

It's another example of the Plessey practice of giving your mini a great deal more capacity and flexibility for a great deal less.

The PM-716 augments our line of miniperipherals, which includes DEC and NOVA add-on memories, dual disc drives and controllers at big savings, and high performance photo-electric paper tape equipment, as well as a powerful 16-bit microprocessor (MIPROC 16).

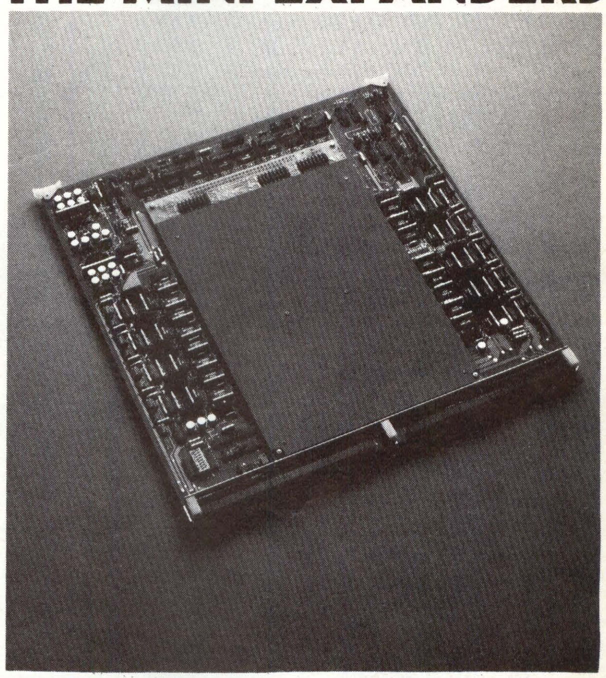
Contact us today for details or a demonstration. Whatever you need, you're going to be impressed by what we can do for your minicomputer system.

And love what we can do for your budgets.

PLESSEY
MICROSYSTEMS
(714) 540-9945

CIRCLE 8 ON INQUIRY CARD

THE MINI EXPANDERS



THE PLESSEY PM-716

CALENDAR

CONFERENCES

Oct 14-16—IEEE Semiconductor Test Sym, Cherry Hill Inn, Cherry Hill, NJ. **Information:** Miss Helen Yonan, Phila Sec IEEE, Moore School of Eng, U of Pennsylvania, Philadelphia, PA 19174. Tel: (215) 594-8106

Oct 16-18—Nat'l Conf on Solid-State Power Conversion, New York Hilton, New York City. **Information:** Ron Birdsall, Conf Chrmn, Powercom, Inc, 2323 Roosevelt Blvd, Oxnard, CA 93030. Tel: (805) 985-2289

Oct 20-30—Data Communications Conf, Iowa State U, Ames. **Information:** Richard Horton, 306C Coover Hall, Iowa State U, Ames, IA 50011. Tel: (515) 294-3131

Oct 21 (Cherry Hill, NJ), **Oct 23** (Long Island, NY), **Nov 20** (Palo Alto, Calif), Invitational Computer Conf. **Information:** B. J. Johnson & Assoc, 300 Otero, Newport Beach, CA 92660. Tel: (714) 644-6037

Oct 27-29—ISHM Technical Sym, Sheraton-Towers Conv Ctr, Orlando, Fla. **Information:** International Society for Hybrid Microelectronics, PO Box 3255, Montgomery, AL 36109. Tel: (205) 272-3191

Oct 28-30—22nd IEEE Machine Tools Conf, Red Carpet Inn, Milwaukee, Wis. **Information:** Robert L. Douglas, Gilman Eng & Mfg Co, 305 W Delavan Dr, Janesville, WI 53545

Oct 28-30—Canadian Computer Show & Conf, Exhibition Pl, Toronto, Canada. **Information:** Derek A. Tidd, Industrial and Trade Shows of Canada, 481 University Ave, Toronto M5W 1A7, Ontario, Canada

Nov 3-5—SEMICON/Europa, Zuespa Conv Ctr, Zurich, Switzerland. **Information:** SEMICON/Europa, c/o Golden Gate Enterprises, Inc, Marina Playa Office Pk, 1333 Lawrence Expy, Santa Clara, CA 95051. Tel: (408) 241-7400; or I. Willener, CH-8001, Zurich, Lindenstrasse 33, Switzerland

Nov 11-14—12th Electrical/Electronics Insulation Conf, Sheraton Boston Hotel/Hynes Audit, Boston, Mass. **Information:** E/EIC, PO Box 159, 700 Peterson Rd, Libertyville, IL 60048

Nov 18-20—Microcomputer Application Workshop, Islandia Hyatt Hotel, San Diego, Calif. **Information:** William J. Dejka, Code 4050, Navy Electronics Laboratory, San Diego, CA 92152. Tel: (714) 225-6454

Nov 19-20—IEEE Computer Soc Sym on Computer Arithmetic, Dallas, Tex. **Information:** Prof D. E. Atkins, Dept of Elec and Comp Eng, U of Michigan, Ann Arbor, MI 48104. Tel: (313) 763-0038

Dec 1-3—IEEE Internat'l Electron Devices Meeting, Washington Hilton Hotel, Washington, DC. **Information:** Institute of Electrical and Electronics Engineers, 345 E 47th St, New York, NY 10017. Tel: (212) 752-6800

Dec 1-3—IEEE Nat'l Telecommunications Conf, Fairmont Hotel, New Orleans, La. **Information:** Institute of Electrical and Electronics Engineers, 345 E 47th St, New York, NY 10017. Tel: (212) 752-6800

Dec 9-12—21st Annual Conf on Magnetism and Magnetic Materials, Benjamin Franklin Hotel, Philadelphia, Pa. **Information:** Conf Chrmn, R. L. White, 124 McCullough Bldg, Stanford University, Stanford, CA 94305; or Local Comm Chrmn, B. Stein, Univac div of Sperry Rand, PO Box 500, Blue Bell, PA 19422

Dec 11-12—CECC/CEDPA (Calif Educational Computer Consortium/Calif Educational Data Processing Assoc) Joint Conf and Trade Show, International Hotel, Los Angeles Airport, Calif. **Information:** Ellen Landers, Show Mgr, 1975 CECC/CEDPA, 17123 Chatsworth St, #10, Granada Hills, CA 91344. Tel: (213) 360-2786

Jan 19-21—2nd Annual Sym on Computer Architecture, Fort Harrison Jack Tar Hotel, Clearwater, Fla. **Information:** Oscar N. Garcia, U of South Florida, College of Eng, Tampa, FL 33620. Tel: (813) 974-2581

Jan 20-23—Computer Soc of India Annual Conv, Hyderabad. **Information:** DVR Vithal, Prog Chrmn, CSI 75 Computer Group, Tata Institute of Fundamental Research, Bombay 400 005, India

Jan 29-30—3rd Internat'l Congress on Computers in Industry, Hotel Hilton, Paris, France. **Information:** P. Daudier de Cassini, Institut d'Informatique et de Gestion, Insig-5, rue Quentin-Bauchart, 75008 Paris, France

Feb 18-21—IEE 2nd Internat'l Conf on Telecommunication Switching Systems, Kongresshaus, Salzburg, Austria. **Information:** Annemarie Cunningham-Swendell, Institution of Electrical Engineers, Savoy Pl, London WC2R 0BL, England

SEMINARS

Oct 29-31—Computer Performance: Measurement and Evaluation, U of Wisconsin, Milwaukee. **Information:** John M. Leaman, Prog Dir, Dept of Eng, U of Wis-Ext, 929 N Sixth St, Milwaukee, WI 52303. Tel: (414) 224-4189

Nov 10-12 (Washington, DC), **Nov 17-19** (Atlanta, Ga), **Dec 8-10** (Dallas, Tex), **Dec 15-17** (San Francisco, Calif)—Planning and Designing Distributed Data Processing Systems for SDLC and SNA. **Information:** Saroj K. Kar, Telecom Computer Technology, 599 N Mathilda Ave, Sunnyvale, CA 94086. Tel: (408) 735-9990

Nov 13—Annual IEEE New Orleans Sec Seminar, Fountainbleau Hotel, New Orleans, La. **Information:** G. Allan Ledbetter, South Central Bell, 1215 Prytania St, Rm 505, New Orleans, LA 70140. Tel: (504) 529-8536

SHORT COURSES

Oct 21-23 (Chicago, Ill), **Oct 28-30** (Washington, DC), **Nov 11-13** (Oakridge/Knoxville, Tenn), **Nov 18-20** (Denver, Colo)—Microprocessor Design Courses. **Information:** Pro-Log Corp, 852 Airport Rd, Monterey, CA 93940. Tel: (408) 372-4593

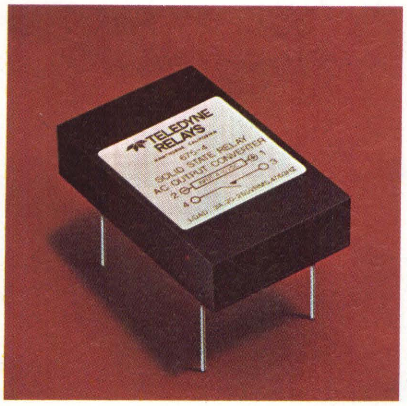
Oct 24-25—Integrated Project Control, Rodger Young Audit, Los Angeles, Calif. **Information:** IEEE Los Angeles Council Office, 3600 Wilshire Blvd, Los Angeles, CA 90010. Tel: (213) 387-1203

Nov 2-7—System Design Using Micro/Minicomputers, Minicomputers—Principles and Applications, Microcomputers—Principles and Applications, Pheasant Run Lodge, St. Charles, Ill. **Information:** National Engineering Consortium, Inc, Oak Brook, IL 60521. Tel: (312) 325-5700

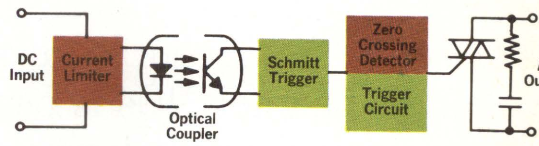
Nov 10-14—Modern Data Communications, **Dec 1-2**—Minicomputer Programming and Interfacing Techniques, **Dec 1-3**—Digital Image Processing of Earth Observation Sensor Data, **Dec 3-5**—Engineering Applications of Minicomputers, George Washington U, Washington, DC. **Information:** Dir, Continuing Engineering Educ, George Washington University, Washington, DC 20052. Tel: (202) 676-6106

Our PCB relays stack the cards in your favor.

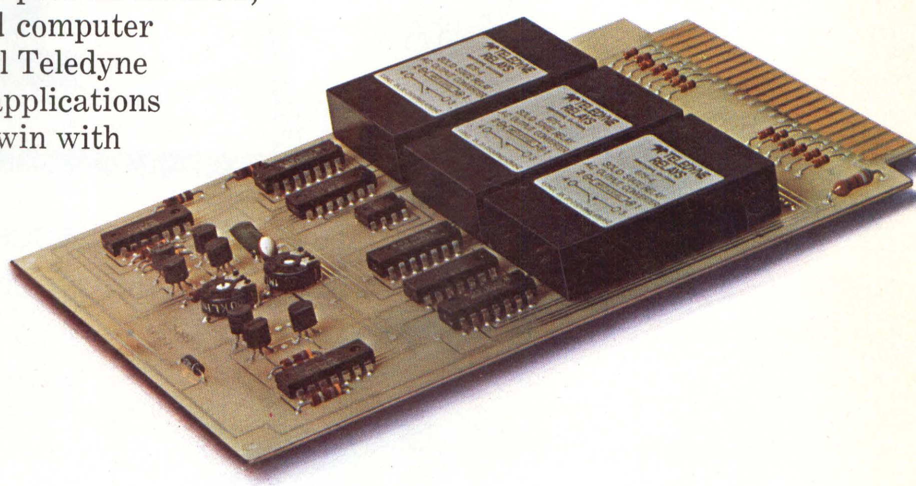
NEW



When it comes to tightly spaced pc boards, you can't lose with Teledyne's new low-profile solid state AC relays. These 0.50 in. (max.) modules are ready-made for direct pc board mounting — making them a sure bet to replace discrete circuits for close center-to-center card spacing. What's more, our low-profile AC relays are optically isolated to provide 1500V RMS isolation to protect logic lines from ac power circuits. Add to this zero voltage turn-on and a high dv/dt capability, and you're sure to beat the odds against RFI and false triggering. Designed for a maximum load of 3 amps at 250V RMS, our PCB low-profile relays come in two logic compatible input voltage ranges: 4-10V DC (model 675-4), and 10-32V DC (model 675-5). In short, they're your best choice for superior packaging and economical solid state switching circuitry for machine tool and process controls, programmable controllers and computer peripherals. Contact your local Teledyne Relays people for full data or applications help. They'll show you how to win with our PCB relays.



Functional Diagram



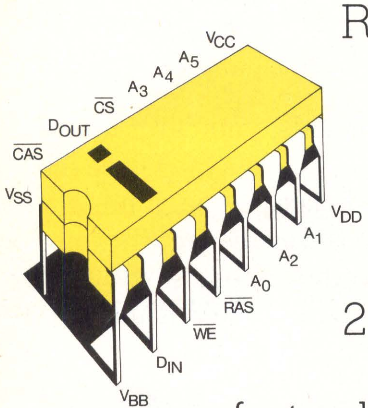
TELEDYNE RELAYS

3155 West El Segundo Boulevard, Hawthorne, California 90250
Telephone (213) 973-4545

CIRCLE 9 ON INQUIRY CARD

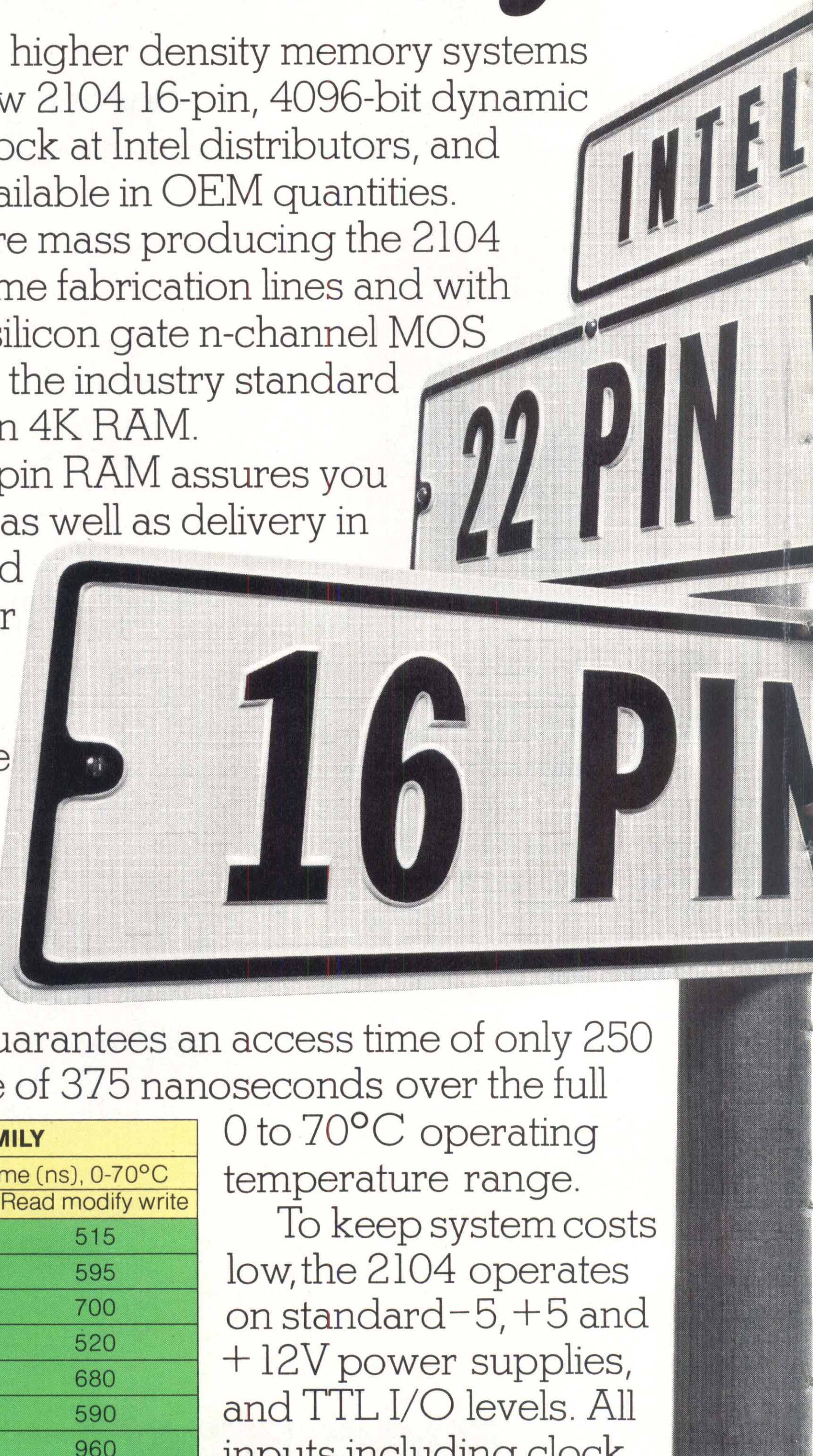
Intel is the way to

You can go into production of higher density memory systems confidently now that Intel's new 2104 16-pin, 4096-bit dynamic RAM is in stock at Intel distributors, and readily available in OEM quantities.



We are mass producing the 2104 on the same fabrication lines and with the same silicon gate n-channel MOS process as the industry standard 2107B 22-pin 4K RAM.

Intel's 16-pin RAM assures you fast, reliable parts as well as delivery in volume. The Intel 2104 is based on the proven single-transistor cell design of the Intel 2107B, the highest performance 22-pin 4K MOS RAM. Like the 2107B, the 2104 chip is much smaller than other 4K RAM chips produced today.



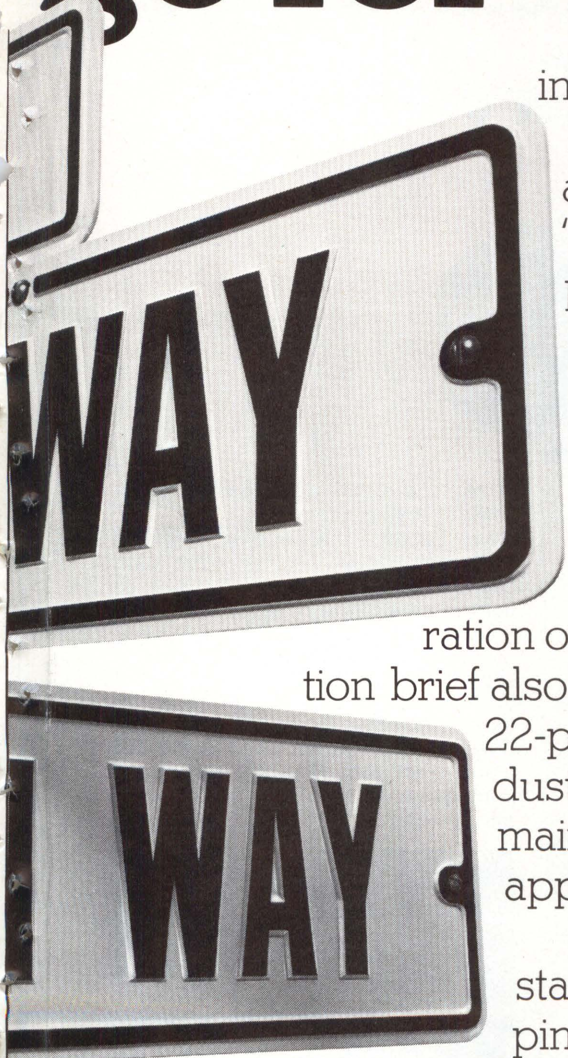
The fastest available 16-pin 4K RAMs are also in the 2104 series. Our 2104-2 guarantees an access time of only 250 nanoseconds and a cycle time of 375 nanoseconds over the full 0 to 70°C operating temperature range.

INTEL'S STANDARD 4K RAM FAMILY

Part Number	Pins	Max. Access Time (ns), 0-70°C	Min. Cycle Time (ns), 0-70°C	
			Read or write	Read modify write
D2104-2	16	250	375	515
D2104-4	16	300	425	595
D2104	16	350	500	700
2107B	22	200	400	520
2107B-2	22	220	470	680
2107B-4	22	270	470	590
2107B-6	22	350	800	960

To keep system costs low, the 2104 operates on standard −5, +5 and +12V power supplies, and TTL I/O levels. All inputs including clock

go for 4K RAMs.



inputs are fully TTL compatible.

Overall system advantages of the 2104 are detailed in a new application brief, "Which Way for 4K... 16, 18, or 22 Pin?" It explains why the 16-pin 2104 is best for very compact systems such as minicomputers, microcomputers, terminals, business equipment, scientific calculators and anywhere high density is needed.

Moreover, we show how the 16-pin standard is compatible with the next generation of even higher density memories. The application brief also tells why the 2107B's simple, straightforward 22-pin design has become an industry standard for computer main memories and many other applications.

NO WAITING 24 HOUR DELIVERY

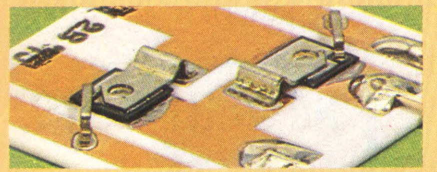
Now the industry has two standard configurations—16 pins with multiplexed addresses and 22 pins with parallel addresses. Whichever way you go, you'll find Intel ready to support both in volume production. For delivery of the 2104 or 2107B contact our franchised distributors: Almac/Stroum, Component Specialties, Cramer, Elmar, Hamilton/Avnet, Industrial Components, Liberty, Pioneer, Sheridan or L.A. Varah.

For your copy of "Which Way for 4K..." or data sheets on any of our 4K RAMs write: Intel Corporation, 3065 Bowers Avenue, Santa Clara, California 95051.

intel® delivers.

Why do more than half the people in the world who buy solid state relays choose Crydom?

Maybe it's because Crydom pioneered, perfected and patented electro-optical isolation and zero-voltage switching. Or because we use efficient back-to-back SCR's. Possibly it's because we offer more standard models. Could be our encapsulation process, our broad distribution, our extensive applications experience, or the fact that you can specify a Crydom relay in the U.S. and order the same part number anywhere in the world.



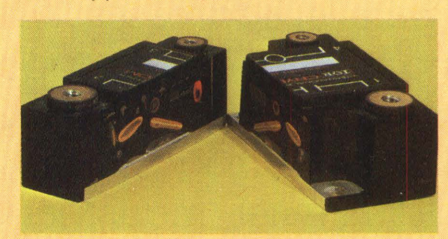
Back-to-back SCR's are superior to triacs in many applications.

Technically Speaking . . .
All Crydom Solid State Relays use inverse parallel SCR's which are superior to triacs in many applications. Back-to-back SCR's have much higher critical dv/dt ratings and greatly improved performance with inductive loads . . . minimal need for "snubbers" or softening devices.

Crydom was the first to use transfer-mold encapsulation, applied under pressure, to fully protect circuitry from humidity, shock & vibration. Many merely "pour fill"—a process that can leave troublesome voids or bubbles within the relay.

Two more firsts. Crydom's patented photo-isolation & zero-voltage switching! The optical isolator, which never wears out, provides complete input isolation without transformers or reed relays. The zero-voltage switching feature minimizes current surges & RFI noise caused by arcing contacts.

Every Crydom relay is 100% solid state. There are no moving parts to malfunction or wear out. This means infinite life, silent operation & no maintenance. Also, Crydom's SSR's are digital logic IC compatible. UL & CSA approved too.



Cutaway photo shows complete encapsulation of components.

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CIRCLE 11 ON INQUIRY CARD

by John E. Buckley
Telecommunications Management Corp
Cornwells Heights, Pa.

Domestic Communications Satellite System

On Apr 13, 1974, the first U.S. domestic communications satellite was placed into a synchronous orbit around the Earth. The operational status of that satellite was symbolically inaugurated on July 15, 1974, when the message originally tapped by Samuel F. B. Morse on the initial telegraph system (in 1844) was transmitted between New York City and Los Angeles. Though these cities are less than 3000 miles apart, the words "what hath God wrought" traveled over 45,000 miles via this Westar I domestic satellite. This event opened the age of domestic satellite-derived communications channels, which is destined to exert great impact and influence on present and future information systems.

The nature of satellite communications systems has been discussed in past columns; those of July and December 1971 presented the results of a series of reliability and error rate measurements that had been conducted by Communications Satellite Corp (Comsat) on a series of international satellite-derived channels. The excellent reliability profile discussed has been substantiated numerous times by data communications users. Indicative of this high reliability is the fact that a number of U.S. data communications users are successfully exchanging data with directly dialed European locations. From U.S. areas where direct European dialing is provided, virtually all of the available communications channels are satellite derived. User experience has indicated that using these direct-dialed links, the quality of data transmission to Europe in many cases exceeded that of domestic data transmissions.

Prior to July 1974, the only communications channels available for U.S. domestic data transmission were the traditional land-based facilities, providing the common resources for leased or switched, voice or data communications services. Since mid-1974, the advantages of a domestic satellite system for all 50 states has become evident to an increasing number of domestic users.

The development of a domestic satellite system was initially given a priority below that of implementation of an international communications satellite system; it was natural that reliable, high capacity transmission paths be established between continents before intracontinental communications needs could be addressed. Nations with large land masses naturally turned to this lower cost and more reliable method of improving communications facilities. In 1965 the Soviet Union launched Molniya I—the first of a number of domestic Soviet communications satellites. In 1972, the first North American communications satellite—ANIK I—was launched, being placed in synchronous geostationary orbit for Telsat-Canada for Canadian use. Although Western Union filed application with the Federal Communications Commission (FCC) as early as 1966 for permission to build a domestic U.S. system, authority to do so was not issued until July 1970.

In August 1972, Western Union contracted with Hughes Aircraft to build three HS333A communications satellites. Two of these were launched in 1974, while the third is being kept as a ground spare to be launched if either of the two operational vehicles should fail, or to meet increasing traffic loads. Initially, five earth stations have been implemented, with New York City, Atlanta, Chicago, Dallas, and Los Angeles comprising the associated major metropolitan areas. These earth-station locations are configured at the logical junction points of the Western Union land-based microwave network. Each Westar satellite has 12 independent amplifiers with a bandwidth of 36 MHz each. Each amplifier has the capacity of 1200 4-kHz voice-grade channels.

The Westar Satellite system is available to other communications common carriers. Domestic satellite-derived channels can be obtained from Western Union or other carriers, such as Microwave Communications, Inc or Southern Pacific Communications Corp. In addition, the interconnection policies of Western Union regarding privately owned systems are quite liberal. Applicable tariffs make these long-distance resources readily available to potential users via a number of methods. With respect to customer access, the Westar system cannot, under any circumstances, be considered an exclusive-Western Union system.

The facilities of this system are presently limited to leased-line services. While these long-distance channels can be technically interfaced to circuit-switching equipment, offerings to date have not encompassed the dial services of the various communications common carriers. The result of this configuration limitation is the predictability of transmission characteristics, particularly with respect to propagation time. An information system user will not encounter a satellite-derived channel unless the interconnecting circuit has been explicitly ordered to include a satellite segment. It is quite reasonable to expect, however, that confinement of satellite-derived channels to leased services will be short-lived. It is considerably less expensive for the communications common carrier to use a satellite-derived than a land-based channel.

The extent of this cost differential can be fully appreciated by comparing the channel costs of leased lines between New York City and Los

Angeles. A land-based AT&T channel under the High-Low Tariff (FCC 260) would incur a typical monthly cost of $2181. The same channel between the New York City and Los Angeles earth stations is tariffed at $1000. Similar long-distance channel cost savings are experienced between New York and Dallas ($750) and New York and Chicago ($500); comparable land-based channel costs are $1223 and $635, respectively. These comparisons are for earth station to earth station equivalent channels; costs of land-based channels between user locations and the nearest earth stations are additive.

While the use of satellite-derived channels is economically beneficial, other characteristics may create advantages or disadvantages, depending on the nature of the specific data communications application. Due to the limited number of present earth stations (five), the cost of leasing land-based channels between the various data terminal or multiplexer locations and their nearest earth stations for a specific information system configuration could negate potential cost savings. Each application must be carefully evaluated and comprehensive network cost comparisons developed to properly define any economic advantages.

The transmission error rate potential of a satellite-derived channel is considerably more favorable than comparable rates experienced on land-based channels. At least a 2-order-of-magnitude improvement has been measured by Comsat on international channels, and an additional order of magnitude beyond this has been measured on Westar channels. Regardless of the exact statistics measured for specific error rate tests, considerably higher quality channels are characteristics of this satellite system than traditionally experienced on land-based channels. The information system user, however, must recognize that these statistics relate to channels between earth stations. Unfortunately, all user locations cannot be co-located with the earth stations. Therefore, the use of land-based channels between user locations and the nearest earth station is required. The only meaningful error rate statistic will reflect the entire circuit's error rate, which will equal that of the poorest quality segment, ie, the land-based channel segment. Unfortunately, the high quality characteristic of the satellite-derived channel will have no influence on the associated information system's performance.

The most visible and yet unavoidable characteristic of a satellite-derived channel is its inherent propagation time. Since the satellites are in an orbit of 22,500 miles, total channel mileage between earth stations is approximately 45,000 miles. At the speed of light, the propagation time equals approximately 242 ms (with round-trip propagation equivalent to 484 ms). It is reasonable to estimate that an actual signal will propagate more slowly than light. When delays of the associated land-based channel segments are added, the system designer must recognize that while a lower channel cost may be realized, the associated transmission timing and protocol may be significantly impacted so as to result in considerably reduced data throughput or even total non-operation of the various data terminals. The promise of an improved error rate is primarily illusionary. A higher quality channel will be experienced between earth stations; however, the poorer quality land-based channels will actually dictate overall circuit quality.

The launching of additional domestic satellite systems is being actively planned by a number of common carrier and even private organizations. Both AT&T and MCI have applications pending before the FCC. The increase in the number of major earth stations as well as the ability to integrate a distributive concept is rapidly being developed. Such a concept accepts a number of small, low capacity earth stations to focus directly on the orbiting satellite, thereby eliminating the need for land-based channels between a user location and the nearest earth station. One of the first applications of this approach is the direct interconnect of off-shore drilling platforms via the Westar satellite.

The age of satellite communications is rapidly maturing, with higher quality data transmission at lower cost the immediate result. This, however, can be realized only by implementing certain adjustments in traditional information system operating characteristics. Today, the use of satellite-derived channels is optional; tomorrow, such channels will be mandatory. □

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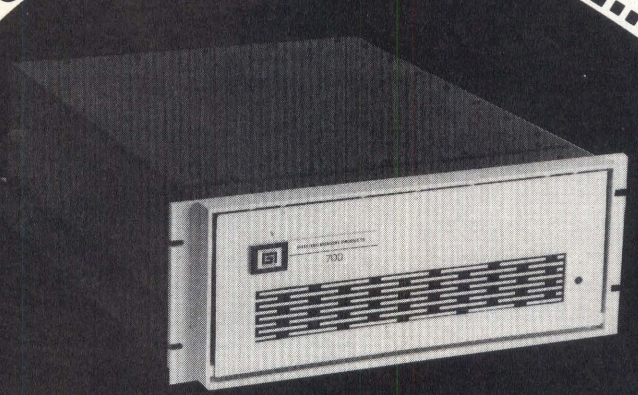

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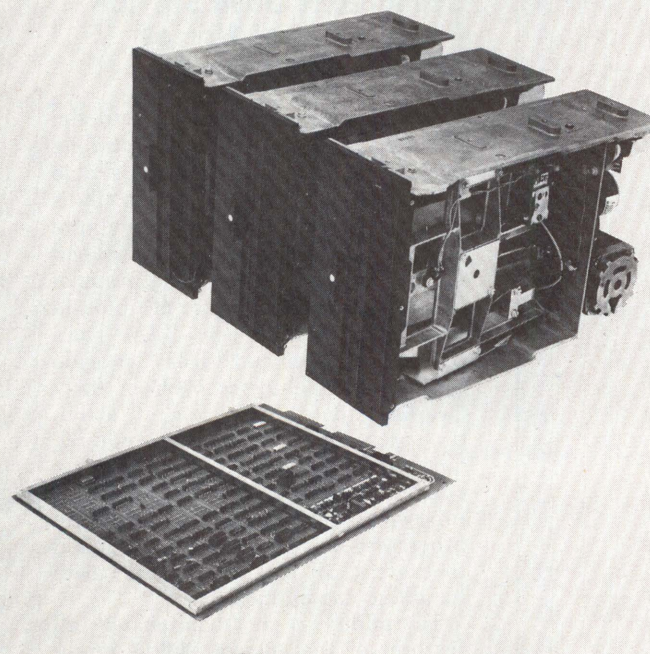
The Streaker...

Introducing the Nude "38" hundred



The "Streaker"... what it's all about. First of all it is a stripped down version of our perfect "38" hundred Diskette Storage Subsystem. The new SA8800 "Streaker" Kit consists of a single 12.5 inch by 17.5 inch PCB disk controller and from one to six diskette drives operating at single or double density.

The "Streaker" Kit is ideal for OEM's who wish to include their own "value added" features. You can add your own cabinet, power supply, and interface. Or, if you wish, you can purchase a standard Shugart SA3800 Diskette Storage Subsystem and add additional drives in increments of one, two, or three in a single cabinet. The SA3800 contains from one to three SA800 drives, the PCB controller board and power supply, all in one package.

The "Streaker" controller board handles up to six drives in the IBM 3740 format (3.2 megabits per drive) or in the double density format (6.4 megabits per drive). The controller board performs all of your required functions including formatting, serializing / de-serializing, seeking and error detection. All that is required to implement the "Streaker" into your system is an interface that you design to meet your system specifications.

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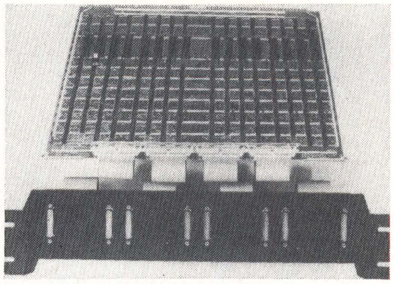
CIRCLE 12 ON INQUIRY CARD

Synchronous Capability Added to Programmable Data Channel Multiplexer

Reception and transmission of synchronous data at any speed up to 50,000 baud as selected by a system modem can be attained by the EDS-302 multiplexer. Configured as one 15 x 15" add-on card for the series of cards in the company's EDS-8 programmable data channel multiplexer, all of which plug into spare slots in Nova type computers, the -302 expands capability of the -8 to include up to eight synchronous channels (by increments of two ports) in addition to as many as 120 existing asynchronous channels.

Operation can be in automatic buffer mode through the computer's DMA channel. In this mode, character strings are transferred via the data channel into or out of buffer areas in core memory. Since size and location of the buffers is under software control, entire message frames can be transmitted or received without any interruption of the computer program.

Hardware generates the cyclic redundancy check (CRC) code, and checks the data; the code is superior to use of just a parity bit in ensuring data integrity. Moreover, its implementation in hardware (rather than in software) reduces the computer's I/O processing overhead.



EDS-302 multiplexer is built on a single card that plugs into a spare slot in Nova type computers. As many as eight synchronous ports can be included (in increments of two)

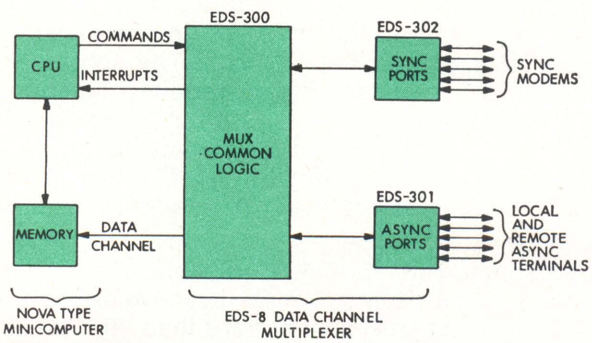
Synchronous ports are compatible with the ADCCP standard as well as SDLC and HDLC. Flag sequence, zero-bit insertion/extraction, and frame check sequence are implemented in hardware; address, control, and information fields are under software control.

All data and control lines operate in accordance with EIA RS-232-C, in either full- or half-duplex modes. Outgoing data set control lines (request to send, data terminal ready, and secondary request to send) are under program control. Five incoming data set control lines (clear to send, data set ready, ring indicator, received line signal detector, and secondary received line signal detector) are available to the programmer.

Only interboard and multiplexer-to-computer signals are routed through the computer harness. Lines from all -8 boards to the communications system are routed directly via ribbon cables. This enables the multiplexer to circumvent the pin limitations of the computer connectors, and also provides flexibility in the computer configuration itself.

Price of the EDS-302, made by Educational Data Systems, 17981 Sky Park Circle, Irvine, CA 92707, with eight synchronous channels is $3600. A 2-channel version is $1200. Total cost of a complete EDS-8 multiplexer system including eight asynchronous channels, two synchronous channels, all necessary cables, connectors, junction panels, and power supply is $4430 for a single unit. Quantity discounts are available. Delivery is 30 days ARO.

Circle 140 on Inquiry Card



Capabilities of Educational Data Systems' EDS-8 data channel multiplexer are expanded by the EDS-302 to include eight synchronous channels in addition to as many as 120 existing asynchronous ports. Synchronous data can be received and transmitted at speeds up to 50,000 baud

Standalone Data Station Features First Use of Mini Data Cartridges

The first product to incorporate the miniaturized 3M data cartridge, model 2644A CRT terminal is able to perform on a standalone basis many operations that normally require connection to a computer. Described as a "mini data station," the terminal contains 220,000 bytes of built-in mass data storage on RAMs and p/ROMs. Mini-cartridges provide storage—115,000 bytes each—of daily "working" data. Control of all activities—program preparation, editing, tape copying, and tape-to-printer operations—is maintained by a microprocessor. A sufficient range of microprogrammed instructions is included to exercise all of the terminal's data handling capabilities.

In addition to maintaining all features of the current 2640A terminal, the 2644A—announced by Hewlett-Packard Co, 1501 Page Mill Rd,

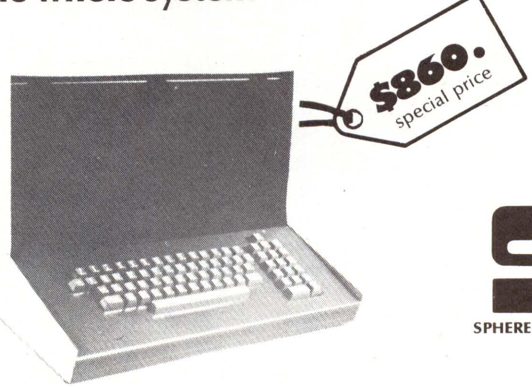
You'll get more than a core.

We make the difference count.

A completely intelligent micro-system . . . that's what we offer, and look at the price! No compromising, no short cuts, no bluff—a one-card computer, it's possible by truly innovative micro-circuit design. The 4K memory capability is built-in, along with a real-time clock to provide for monitoring capabilities. SPHERE SYSTEMS can be programmed with full extended BASIC, plus the intelligent terminal is totally compatable with existing high-performance, low-cost perpherials (also available through SPHERE) which make your possibilities almost limitless!

We're talking about the lowest-cost complete systems around. Contact us for more information about our one-card computer, or a most complete line of peripherials and software support. At SPHERE CORPORATION, we make the difference count.

the whole system



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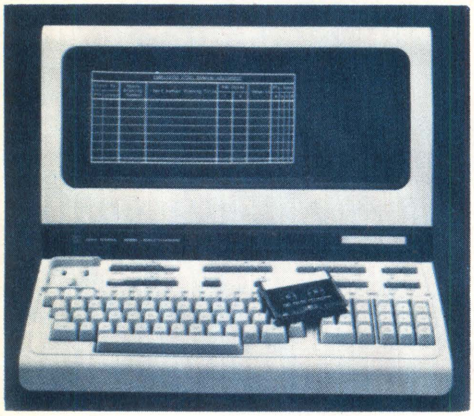

Hewlett-Packard's microprocessor-controlled CRT terminal can perform as a standalone "mini data station." Two 3M mini-cartridges, used here for the first time in a product, fit into tape transports located in the front of the display unit. (One mini-cartridge is shown on the keyboard; the rear of the other is the white rectangle just above the right end of the keyboard.) 220,000 bytes of mass data storage are built into the terminal and each mini-cartridge holds 115,000 bytes

Palo Alto, CA 94304—attains its standalone capability through microprocessor control and two fully-integrated tape transports for the mini data cartridges. In data entry, for instance, forms stored on one mini-cartridge can be selectively retrieved in seconds for display on the CRT. Data can then be entered to the display from the keyboard. Entry of data is eased by features such as protected fields, video highlighting, and elaborate editing capability. Once confirmed, the entered data can be stored on a second mini-cartridge by pressing a single button. Full mini-cartridges can be batch transmitted to a computer system at the end of the day's work or whenever practicable.

Single keys execute the most common tape data transfer commands. Touching one of eight "file" buttons automatically calls up the appropriate one of the first eight files on a cartridge; typically these are forms. "Read" and "record" are single-button functions.

Two prefix keys speed operations. Input/output functions are assigned by first touching a green prefix key, and then the appropriate input and output device keys. Data may be moved readily among any of the station's functional units, between cartridge tapes, from the keyboard, to or from the display's semiconductor memory, to a printer, or to or from the RS-232-C data communications interface.

A gold key is the prefix for quick access to extended operations. For example, pressing "gold key + find file key + file-number key + cartridge ident key" calls up any of 255 files at search speed (60 in./s). File records may vary in length from 1 to 256 bytes, stored in ASCII or binary format.

The shirt-pocket size (3 x 2½ x ½") mini-cartridge is reported to have longer life and better interchangeability than the company has experienced with cassettes. In the 2644A application, 115,000 bytes of serial information are recorded single-track on each cartridge, using the full 0.15" width of the mini-cartridge's 140 ft of tape at a density of 800 bits/in. Tape speed is 10 in./s; therefore transfer rate to or from the display is up to 8000 bits (1000 bytes)/s. Since search is at 60 in./s, average access time is 10 s. One cartridge contains the equivalent of 1000 ft of paper tape.

Within the enhanced 5 x 10" CRT display, 1920 characters (9 x 15 dot cell) can be presented in a 24-line by 80-col format. Inverse video (black on white), blinking, half-bright, and underlining may be employed in all of 16 possible combinations. Multiple character sets can be displayed. A 128-char Roman set, including lower case and displayable control characters, can be used along with as many as three additional character sets. A math-symbol set and a line drawing set, to generate user's entry data forms, are available.

Full editing capability is provided to correct data before transmission or recording. Standard features include character and line insert and delete, cursor sensing and positioning, programmable protected fields for forms, off-screen solid-state memory storage with scrolling and page-select, tabulation, eight special-function keys for user-defined routines, and a positional memory lock. The terminal uses an ASCII RS-232-C communications interface and can transfer from semiconductor memory at rates up to 2400 baud (9600 baud on binary output).

Circle 141 on Inquiry Card

Subsystems Expand Capabilities of Computer Series

Announced by the Sperry Univac division of Sperry Rand Corp, PO Box 500, Blue Bell, PA 19422 for use with its 90/60 and 90/70 computer systems, three subsystems meet the requirements of widely diverse users. A multichannel communications controller (MCC) increases benefits of communications control and provides a simplified method of modifying a network; a magnetic tape subsystem, Uniservo™ 14, offers non-return to zero inverted (NRZI) or phase-encoded (PE) recording (or both in dual density version); and two disc drives—a fixed-head unit, 8405-00, for real-time applications, and a removable disc system, 8433, for handling large data bases—provide faster access times and transfer rates. All function under Virtual Memory Operating System/9 (VS/9).

Multichannel Communications Controller

MCC combines the design principles of the 3760 controller with VS/9 software to expand the communications capability of the series 90 computers. It emulates and provides full functional capabilities of the earlier communications controller multichannel (CCM). Improvements include support of more high speed lines as well as a mix of line speeds, disciplines, and protocols—including both Univac and industry-standard terminals and high speed computer-to-computer communications.

Peak throughput is increased to a maximum of over 25,000 char/s. Line speeds from 45.5 bits/s to wideband speeds of 56,000 bits/s can be accommodated. MCC can support up to eight line speeds concurrently, and be used with up to 59 lines, depending on the number of subchannel registers available on the host processor. Since MCC uses significantly less power, it dissipates less heat than older equipment.

Three versions are available: model 1 accommodates up to 16 half- or full-duplex lines; dual-scanner model 1A handles an additional 16 lines; and model 2 can be used with up to 59 half-duplex or 29 full-duplex lines. A 32-line version can be housed in a cabinet about the size of a desk. The smallest model MCC can be upgraded in the field to fuller

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digital

CIRCLE 15 ON INQUIRY CARD

capabilities as communications requirements expand.

Applications available in VS/9, and hardware supported with the MCC, include remote job entry or remote batch processing, interactive program development, transaction processing, inquiry/response, data collection, and message switching. Operating under host processor control, MCC performs such functions as character-sequence detection or insertion; code translation; and cyclic-, longitudinal-, and vertical-redundancy character generation on transmitted messages; and checks for such characters on received messages. The controller also performs automatic dialing and answering, and interfaces a wide variety of common carrier lines.

A Test Assistance Program (TAP) allows customer engineers to test individual lines, line adapters, modems, and terminals without interfering with production communications processing. New lines and terminals can be verified without using host processor time or taking all communications offline.

Circle 142 on Inquiry Card

Magnetic Tape Subsystem

Three versions of Uniservo 14 are available: a 9-track unit with PE recording format and transfer speed of 96 kilobits/s; a 7-track unit using NRZI recording format at transfer speeds of 48, 33.4, or 12 kilobits/s; and a 9-track dual density unit that has both PE and NRZI recording formats at 96- and 48-kilobit/s transfer speeds, respectively. Recording densities of the three versions are 1600, 800/556/200, and 800 bits/in., respectively. All operate at 60 in./s.

Automatic tape loading assures ease of operation and maximum operator efficiency. Single capstan drive design of the cartridge uses a minimal number of mechanical parts with resultant reduced tape wear.

Tape units are attached to the system via a type 5045 control unit which incorporates features for dual channel and 7-track operation. A control unit and two tape units are housed in the same cabinet. VS/9 automatically allows the interactive user to temporarily remove certain files from the disc units, when the demand for this space is high, and place them on tape.

Circle 143 on Inquiry Card

Disc Drives

Both the 8405-00 fixed-head disc storage unit and the 8433 removable disc system use the microprogrammed 5039 control unit. The 8405-00 has 8.34-ms average latency, 622-kilobyte/s transfer rate, and 6-megabyte storage capacity on 12 recording surfaces. On the 8433, storage is up to 200 megabytes in free format, 190 megabytes in VS/9 page format. Transfer rate is up to 806 kilobytes/s, average latency is 8.33 ms, and average arm-positioning time is 30 ms. Eight disc units of either type can be attached to a control unit; and eight more can be added by using an F2047 16-drive expansion feature.

Circle 144 on Inquiry Card

Low Cost MOSFET Memory Add-Ons Expand System/3 Efficiency

Add-on semiconductor memory for the System/3 model 10 market is claimed to provide increased system efficiency at up to 70% less cost than IBM core memory. According to Decision Data Computer Corp, 100 Witmer Rd, Horsham, PA 19044, manufacturer of the 5410 System/3 memory, use of the add-ons not only increases the model 10's system capabilities, but also makes it a more attractive system than the recently announced model 12. Savings permit additional memory to be used with a model 10 to increase its performance potential through faster sorting, elimination of program overlays, faster I/O through double buffering, and use of larger blocks. In some configurations this could permit communications to be used which were marginally justifiable in the past.

Add-on MOSFET memory is offered in 8-kilobyte increments up to 56 kilobytes. Existing IBM memory must be 8 kilobytes. Memory cycle time is 1.52 μs. No extra power source is required; operation is off the System/3 ac supply. The memory is completely compatible with hardware, operating procedures, and maintenance requirements of System/3 model 10.

Monthly rental prices for the add-on, including memory, range from \$115 (8K) to \$480 (56K). Purchase prices range from \$4800 to \$12,900.

Circle 145 on Inquiry Card

Specialized Processors Ease Communications Data Transfer Problems

Communications processor versions of the MODCOMP II and IV computers, MODCOMP II/CP2 and IV/CP contain all features of the standard models but, in addition, offer a set of hardware-implemented macroinstructions for processing communications data. They also provide a direct memory path for transferring data between processor and communications lines via universal communications subsystem-model 2. Both CP computers and the communication subsystem are manufactured by Modular Computer Systems, Inc, 1650 W McNab Rd, Ft Lauderdale, FL 33309. Data transfer occurs on a block basis without program intervention.

A set of core-to-core byte move instructions added to the standard MODCOMP instruction set permits translation, CRC or LRC accumulation, character insertion, deletion, or replacement to take place during byte transfers. They also permit search for up to eight program-selected characters. Any or all of these options may be activated during a given byte move operation. While the move instructions are implemented using microcode, high overhead functions such as character comparisons and CRC generation are implemented in hardware. This procedure enables the core-to-core move to operate at memory speeds.

Direct memory interface (DMI) for the universal communications subsystem provides 256 full-duplex direct memory access channels to the communications controller. Since the DMI multiplexes transfers to and from memory, all 256 channels may be active simultaneously. In addition to maintaining a memory transfer address and byte count for each line, the DMI provides a special-character detect capability during block transfers. Incoming lines may be monitored for character sequences in addition to single characters. Special-character detection is controlled by a program specified algorithm for each channel, enabling each channel to search for different characters or sequences. Automatic buffer chaining during input or output transfers permits buffer swapping to occur without program intervention whenever a buffer fills or empties, or whenever a special-character sequence is detected during input.

Major differences between the two CP computers are memory size and interface. II/CP2 is expandable to 128 kilobytes of directly addressable memory, with either 800-ns or 1-μs cycle

In data we've got a lot

In fact, MODCOMP today has broader capability in data communications than anyone else in the minicomputer industry.

Processors. A complete range. From small low-cost processors used where high throughput and big memory are not major concerns, but economy is. All the way to the powerful new MODCOMP IV CP, ideal for large networks and on-line terminal inquiry/retrieval systems. Plus a new model of our MODCOMP II CP with lightning-speed throughput for such applications as front end processing, message switching and high speed line concentration.

Memory size. Introduction of the MODCOMP IV CP expands your choice of memory size to a hefty half-million bytes, with an effective cycle time of 500 ns.

Direct Memory Interface. Separate bus provides private direct memory path to the communications subsystem on all CP models.

Four-port memory. An added feature of the MODCOMP IV CP. Allows the communications DMI its own port for transferring data to and from memory without stealing cycles from the central processor.

Macro instructions. Provided in all MODCOMP Communications Processors to permit direct core-to-core byte transfers at memory speed. Several edit options plus code translation can be performed, singly or in combination, during byte moves. BCC computation is executed at no additional cost in byte movement time.

Character Detect hardware. Monitors all input lines for individual characters, sequences or a combination of both.

Buffer chaining. Allows multi-block direct memory transfers without program intervention.

Universal subsystem. A new model of our well-proved communications multiplexer, across-the-board compatible with all MODCOMP II and IV processors. The MUX with a mind of its own, it simultaneously handles up to 256 full duplex sync and async lines. At varying line speeds. In any combination.

PROM-controlled line scanner. Replacing the commonly-used fixed-rate line scanner to handle a wide range of low, medium and high speed lines.

Multiple baud rates. Fifteen separate program selectable baud rates available for each asynchronous line.

Program modem control. Each modem signal may be individually controlled for complete flexibility and modem independence.

Line Interface Modules. Synchronous and asynchronous modules offer total coverage of a wide variety of line connects and modems. Current loop. RS232. Wideband.

MAXCOM. A standardized operating system designed by MODCOMP exclusively for communications systems.

All this is just a sample of MODCOMP's strength.

For more information, write Communications Marketing, Modular Computer Systems
1650 West McNab Road, Ft. Lauderdale, Fla. 33309
Phone (305) 974-1380

European Headquarters:
103 Mytchett Road, Mytchett, Surrey, England
Phone (0252) 514251

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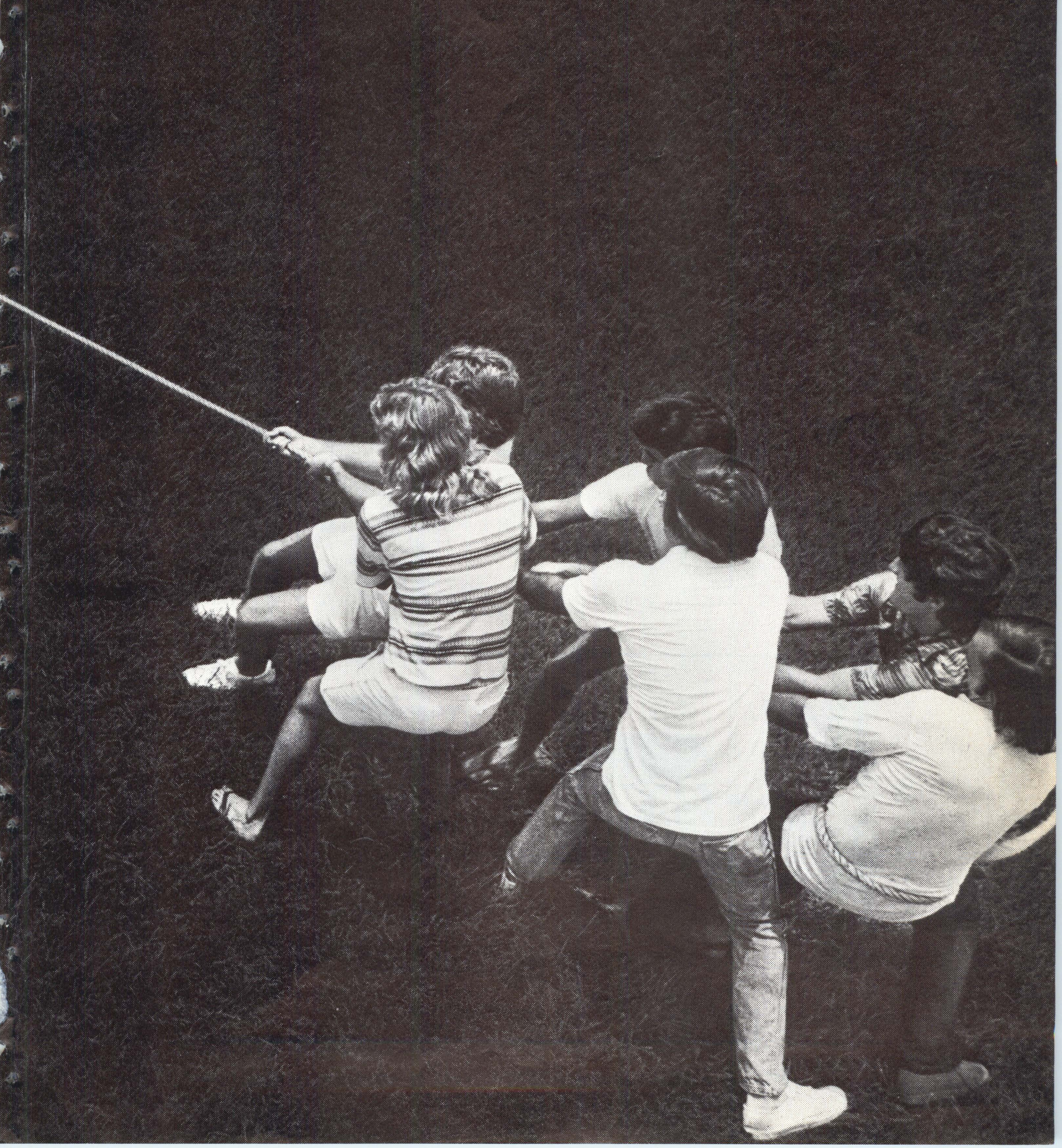
INTERNATIONAL OFFICES OR REPRESENTATIVES IN ENGLAND / FRANCE / BELGIUM / WEST GERMANY / NORWAY / JAPAN

CIRCLE 17 ON INQUIRY CARD

communications, more pulling for us.



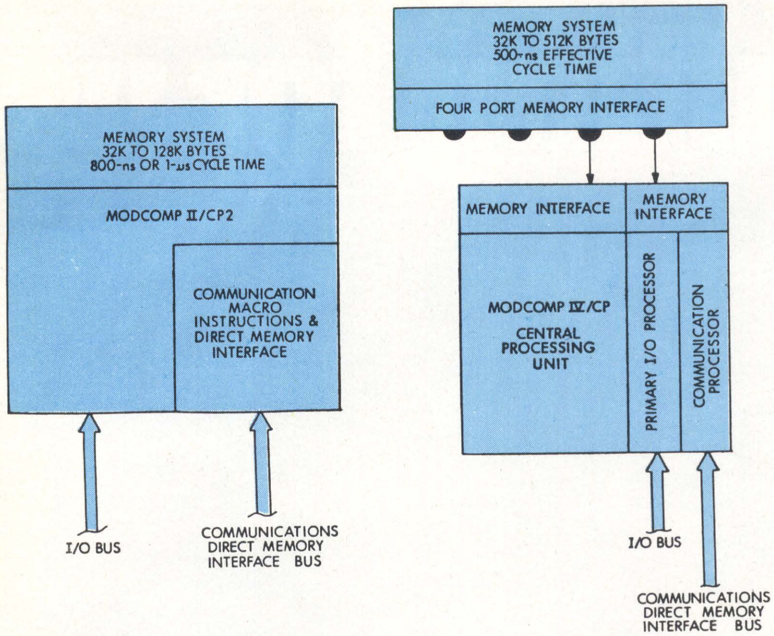


Fig. 1 Direct memory interface (DMI) on MODCOMP II/CP2 communications processor (left) shares memory port with the CPU. However IV/CP DMI (right) transfers data via its own port; it also converts virtual user addresses into physical memory addresses, while allowing sequential data transfers across multiple physical memory pages without program intervention

time; and DMI shares a memory port with the CPU. Memory on the IV/CP is expandable to 512 kilobytes. Basic memory cycle time is 800 ns, but since all memory is interleaved, the effective cycle time is 500 ns. Data are transferred by DMI to and from memory through one of four memory ports, eliminating the need to steal cycles from the CPU.

Primary throughput bottlenecks in a communications system are transferring data between memory and the communication lines, and processing data once in memory. Also, character handling on an interrupt basis permits program control of the processing required for a specific protocol, independent of the hardware. The primary consideration when using direct memory transfer is that of detecting short blocks and of accumulating or generating block check characters in accordance with a specific protocol. If this intelligence is placed in each line interface unit, the cost is increased significantly. The CP computers centralize the special-character sequence logic in the DMI and place only the basic intelligence required to serialize or deserialize data in the line interface units. This results in lower cost for line interface units. The byte string processing instructions provide the mechanism for protocol-dependent processing in an efficient manner without the loss of flexibility.

Universal communications subsystem—model 2 can interface as many as 256 full-duplex synchronous and/or asynchronous lines to any model II or IV processor. Each chassis connected to the universal controller may contain 1 to 16 dual line-interface modules, permitting up to 32 lines per chassis. These lines may be any combination of synchronous and asynchronous.

Universal subsystem controller model 1907 provides all logic necessary to communicate with the attached communications lines. At the heart of the controller is a high speed RAM containing 64 bits of storage for each full-duplex line. Parameters maintained in RAM for each line may be modified by commands from the computer or status changes from the

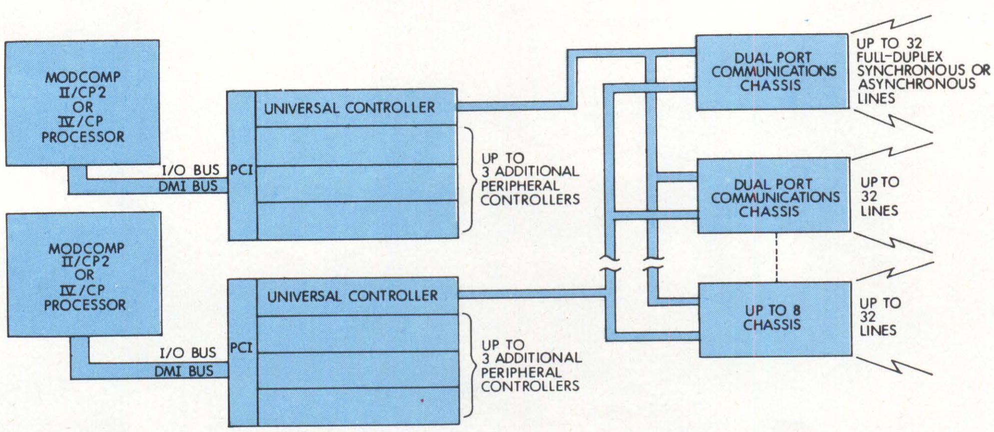


Fig. 2 Redundant universal communications subsystem with communications processors. Dual port chassis may be assigned to only one controller at any given time

line-interface modules. Line scanning is controlled by a p/ROM such that the scan sequence for all lines is controlled by a factory- or user-supplied algorithm enabling high speed lines to be serviced more frequently than low speed lines.

Character buffering between processor and line-interface modules is provided by the controller. Data transfers to and from the central processor use the I/O bus when the controller is attached to standard II and IV processors. These transfers operate under program-controlled (character interrupt) I/O. When the controller is attached to a II/CP2 or IV/CP processor, data are transferred over the DMI in block mode without program intervention.

Universal communication chassis model 1930 contains power, clock source, controller bus interface, and rack-mounting hardware for up to 16 dual line-interface modules. Fifteen separate baud rates are supported by the chassis clock source. Each asynchronous line interface may select one of these 15 rates under program control. Single port models are attached to one universal controller; dual port models may be attached to a pair of model 1907 controllers to provide a redundant configuration. At a given moment, a dual port chassis may be assigned to only one of the two controllers, although it may be switched between them.

Plug-in line interface modules model 193X provide character assembly/disassembly for two full-duplex communications lines. Available in asynchronous and synchronous versions, the modules can be mixed in any given chassis. Asynchronous modules are available for either RS-232 or current-loop lines.

Circle 146 on Inquiry Card

Clustered Terminals Communicate Concurrently in Data System

Claimed to be the lowest priced system of its kind, the Sycor 440 communications system is intended for use in networks with the company's 340 and 350 standalone intelligent terminals. The multi-keyboard, shared-processor system features data entry with concurrent processing and shared files for inquiry-response applications. Announced by Sycor Inc, 100 Phoenix Dr, Ann Arbor, MI 48104, the 440 may be used with the company's proprietary Terminal Application Language, TAL II, to custom tailor data entry with arithmetic operations, conditional data entry, range checking, table look-up, and other intelligent functions.

Communications System

A 440 system includes control unit, up to eight video display terminals, and a variety of peripherals (dependent on user requirements). It can communicate with the intelligent terminals, other 440 systems, or mainframe computers, emulating IBM 2770, 2780, or 3780 protocols.

Each display station operator can access common files to select constant data to support data entry and inquiry/response applications. Concurrently, the system offers background processing including remote job entry, file maintenance (editing, sorting, updating, and file transfer), report generation and multi-terminal printer support to allow each display to interleave data blocks to one printer while data are being keyentered.

The control unit contains system logic memory, device interfaces, power, system control panel, 5- or 10-million-character fixed-disc drive, and either tape cassette or flexible-disc drive to load the fixed disc, store files and system data, or provide a means to interchange data and formats with the terminals. Display on the terminal consists of 576 char on an 8-line x 64-char format with a 64-char status line. Control characters can be blanked out and field labels dimmed with an optional feature. Keyboard may be in either typewriter or data entry (keypunch) styles.

Pricing is $535/mo on a 3-yr lease, $632 on a 1-yr lease, $22,250 purchase for a single-keyboard system; $677, $797, $29,090 for a 4-keyboard system; and $894, $1050, $38,660 for an 8-keyboard configuration. All lease prices include a 5-million-char disc, cassette, communications, and maintenance. Deliveries will begin in the first quarter of 1976.

Circle 147 on Inquiry Card

Enhanced Terminal Application Language

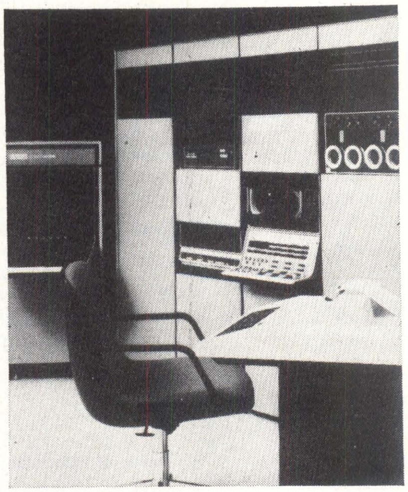
TAL II allows users to write sophisticated application-tailored editing programs. Source program instructions are written in single source statements, omitting separate entries for instructions and tables; and source statements may be given labels and interspersed with comments for program documentation. The source program is entered in a single data stream, eliminating the need for separate tables, groups of field programs, and formats. A listing, produced during program generation, indicates errors in program context if they are present.

A TAL II generator runs without operator intervention once started. Source input is automatic and output is an object program, a generator listing, or both. A TAL-to-TAL II translator operates like a generator. Input is an existing TAL program with its separate tables and groups of field programs; output is an equivalent TAL II source program.

Circle 148 on Inquiry Card

Interactive CAD System Supplies All Drawings For PC Board Design

Most of the preliminary manual layout necessary in designing PC boards with previous computer-aided design (CAD) techniques can now be eliminated. Overall design time in one example can be reduced from 199 hours to only 22 with the Design-a-matic™ interactive graphics design system. Built around a Digital Equipment Corp medium-scale XVM computer configuration and using automated software developed by Redac



Redac Interactive Graphics' CAD system is built around a DEC XVM computer and automated software from Redac Software Ltd. System is claimed to reduce PC board design time to one-tenth that required by standard methods

CIRCLE 19 ON INQUIRY CARD→

Software, Ltd, this CAD system is reportedly priced 25% below previously available systems but provides greater capability. According to Redac Interactive Graphics, Inc, 225 Great Rd, Littleton, MA 01460, it is cost-justifiable for electronic firms that design as few as 75 to 100 PC boards per year.

Design-a-matic can supply all requirements of the PCB design project in a single data base; schematics, assembly drawings, artwork, and drilling tape. It places components (by the Monte Carlo technique), routes the layout for both sides of the board, and checks spacings of lines and components. Depending on software complexity used, it can meet the requirements of commercial, MIL-D-1000 documentation, or DOD microfilm specifications.

Any failures of the system to automatically meet specifications or inability of the software to route lines properly are immediately shown to the operator. Flashes on the CRT indicate problem areas. On such occasions an experienced PCB layout designer solves the problem manually, using a light pen to cancel out incorrect layouts and draw in new ones. The designer can also use the light pen to override the system in seconds if he does not agree with any plot.

A typical full system includes XVM-200 computer with 32K words of core memory, PDP-11 peripheral processor with 8K memory, memory processor, disc and tape mass storage, LA36 DECwriter II keyboard printer, 17" refresh graphics display work station, high speed paper-tape reader/punch, and 12" wet-ink-on-mylar plotter. Larger memories, displays, and plotters as well as other capabilities can be included if the scope of projects requires them.

Normally, a layout process will begin with the PCB designer examining a rough sketch made by the engineer. The designer will then extract basic symbols previously stored in the system's memory from the library and create the missing ones with the light pen. Next, he will position symbols, sub-drawings, identification, and functional blocks of the design and specify interconnections.

Routing of interconnect lines will be performed automatically. Any lines that the system cannot route will appear as point-to-point connections to alert the designer who will then route them properly. When a layout meets all requirements, it can be stored in memory for future use and also reproduced on the plotter.

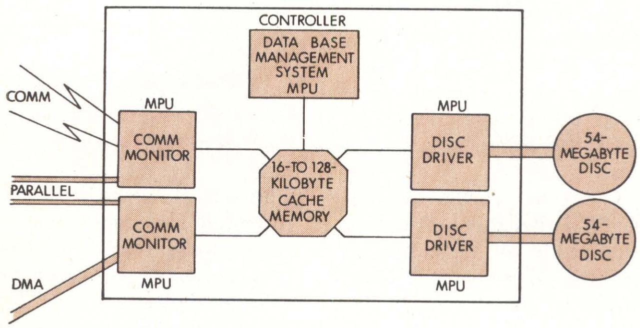
Circle 149 on Inquiry Card

Standalone Intelligent Disc System Reduces Loading on Host CPUs

The "world's first" intelligent disc, intended to remove the load of data base access from the user's CPU, is now available in either 54-megabyte (single spindle) or 108-megabyte (dual spindle) configurations. Made by IMS Associates, Inc, 1922 Republic

Ave, San Leandro, CA 94577, the IMSAI 108 functions as a standalone data base management system accessible by multiple CPUs and/or terminals or as a means to reduce CPU loading while increasing disc capacity. Connection can be by RS-232-C communications or I/O bus parallel interfaces or by direct memory access.

Five interacting disc-controller microprocessors, 16 to 128 kilobytes of 450-ns cache memory, and functionally distributed firmware combine to remove the load of data base access functions from the host CPU. Standard IBM 3336-type discs have 806-kilobyte/s transfer rate and 6-ms max track-to-track access time.



A data base management system, residing in the controller, enables the user's CPUs and intelligent terminals to deal with symbolically named files, records, and fields. Under the data base access protocol imposed by most information storage and retrieval applications, only host commands and specified data field will pass between the host CPU and the disc controllers. All indexing, searching, and deblocking operations are performed by the controller. □

Circle 150 on Inquiry Card

The article on Codex Corp's selective repeat/automatic repeat request (*Computer Design*, Aug 1975, p 18) erroneously states that "Efficiency of satellite channels is degarded by the 600- to 800-ns round-trip delays . . . ." This should have read "degraded by the 600- to 800-ms . . . ."

When it comes to flexibility, the model 40 gives you a lot of ways to go.

When we designed the model 40 system, we included a long list of features and options to give it the flexibility for practically any data transmission requirement. Whatever your industry or application.

First, there's a variety of speeds ranging from 110 to 4800 bps, along with a choice of interfaces, half/full duplex operation and character and batch mode transmission. The model 40 system also has a number of on-line controls, even/odd parity generation and a destructive scrolling feature that permits continuous bottom line reception with no loss of data until memory overflow.

Flexibility features don't stop there, either. There's an expandable memory with line and page scrolling, protected format with variable field transmission, plus many other features and options to select from. And since the entire system is modular, it can be custom-tailored to fit your needs.

These are just some of the many reasons why the model 40 has the flexibility to fit just about any system. But the model 40's strongest suit is economy. Because on a cost/performance basis, nothing even comes close. And delivery is a lot sooner than expected.

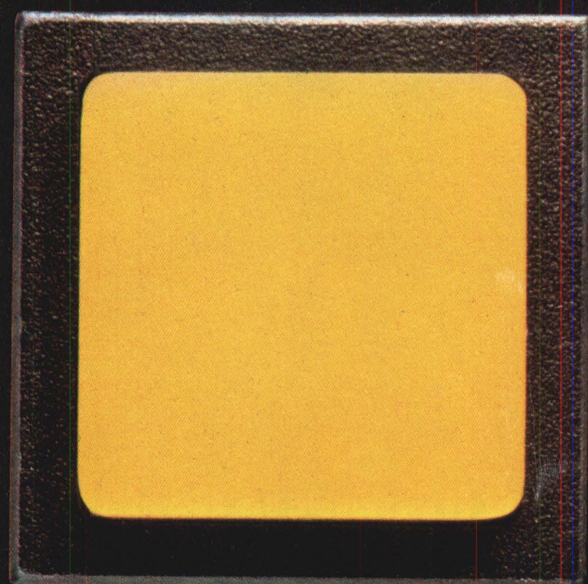
For complete information, please contact our Sales Headquarters at: 5555 Touhy Ave., Skokie, Ill. 60076. Or call Terminal Central at: (312) 982-2000.

TELETYPE ®

The Teletype model 40 system. Nothing even comes close.

CIRCLE 22 ON INQUIRY CARD

Developing this new pushbutton was a little like coming up with a Ferrari that gets 32 mpg, holds 12 people and costs less than a Pinto.

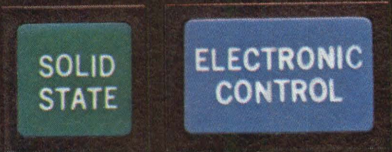


Until now, there have been some good-looking lighted pushbuttons and indicators.

And there have been others with varied electrical capabilities. But there's never been a line that gave you harmonious panel design, electrical flexibility, and low cost. All at the same time. Until now.

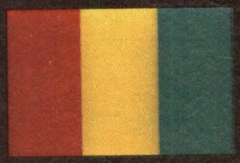
Introducing the MICRO SWITCH Advanced Manual Line—AML.

The most sophisticated line of pushbuttons and indicators ever designed. And you can see a few of



the reasons why right here. The AML button height, bezel size and visual compatability of the square and rectangular sizes "harmonizes" your panel. To give you a panel with a clean, good-looking geometric face. And a panel with increased efficiency, because it doesn't distract. The low-profile square and

rectangular buttons are available in five colors: white, red, yellow, green, and blue. Display capabilities include split screen, hidden color, and a unique three segment lens cap indicator. Illumination can be transmitted or projected. But what you can't see here is what



helps to make these the most advanced line of lighted pushbuttons and indicators available: their extreme electrical flexibility.

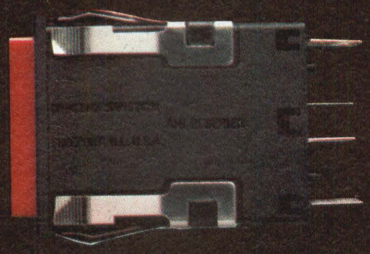
Solid state operates at 5V or 6-16V with a built-in regulator, sink (TTL) and source (CMOS).

Electronic control is capable of handling low energy circuits and has a maximum rating of 3 amps, 120 VAC, with single or double pole double throw.

And power control, DPST, with a rating of 10 amps at 120 VAC.

The AML has snap-in mounting from the front of panel and can also be subpanel mounted. There's a choice of individual or strip mounting.

All devices are the same shallow depth behind the panel to provide a unique single level termination system. The result is ease of wiring and neat appearance.



There are 5 types of terminals available: solder, quick-connect, wire-wrap, push-on or p.c. board mount.

Relamping is accomplished from the front of the panel. And it's done without a tool. With a choice of lamps including a T-1¾ wedge base lamp, neon and LED. To provide international acceptance, every AML device has been designed to comply with essential IEC, CEE24, UL and CSA standards.

For more information on the AML, call your nearest MICRO SWITCH Branch Office. Or write for our literature.

What you'll see is a line of lighted pushbuttons and indicators that give you a completely harmonious panel design in the front.

And the utmost in electrical flexibility behind the panel.

All products shown on this page are actual size.

MICRO SWITCH

FREEPORT, ILLINOIS 61032

A DIVISION OF HONEYWELL

Reader Service Card 23 for data; 24 for salesman call

MICRO SWITCH products are available worldwide through Honeywell International.

World Congress Reports on Developments in Digital Control Technology

A number of papers presented at the International Federation of Automatic Control 6th Triennial World Congress, held in Cambridge, Mass on Aug 24-30, concerned concepts or work in progress that may influence future digital technology. Three typical but diversified papers are abstracted here because of their particular interest.

Space Shuttle Computer Complex

On-board data processing for control, payload management, and performance monitoring of space shuttle orbiter avionics will be provided by five interconnected but independent general-purpose computers—each a modified version of the IBM Advanced System/4Pi model AP-101. During critical phases of a typical mission each computer will perform approximately 325,000 operations/s using floating-point arithmetic.

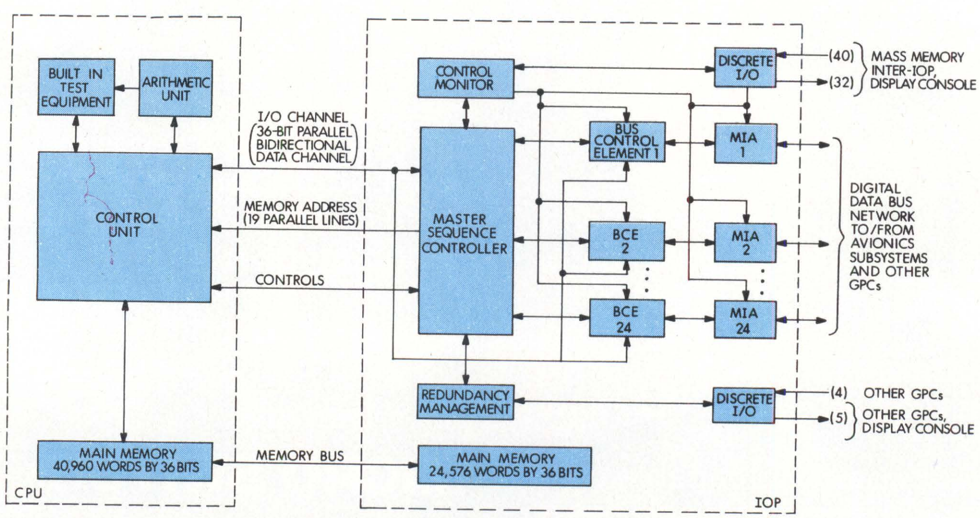
Each computer is made up of a central processing unit (CPU) and an input/output processor (IOP) that operate concurrently. The CPU provides central computational capability and control of interrupts and I/O requests. It processes 480,000 instructions/s, has a 154-instruction repertoire, and operates with 16- and 32-bit fixed-point and 32- and 64-bit floating-point operands. During critical flight phases four computers operate as a cooperative redundant set on guidance, navigation, and control tasks, with the computations of each verified by the others. The fifth handles system management functions.

The IOP controls 2-way data transfer between the computers and other units of the space shuttle over time-shared serial digital data buses and frees the CPU from extensive direct participation in I/O handling. A 36-bit parallel bidirectional data channel provides communication interface between CPU and IOP. Information transfer is by direct I/O when initiated by the CPU and direct memory access when initiated by the IOP.

Microprogramming used for both processors provides flexibility. Each CPU instruction is executed as a series of microinstructions which control CPU hardware, flow of data, and operations performed on the data. The microprogram control unit is made up of a 2K-word x 48-bit monolithic read-only microprogram memory, address register, data register, and decoder.

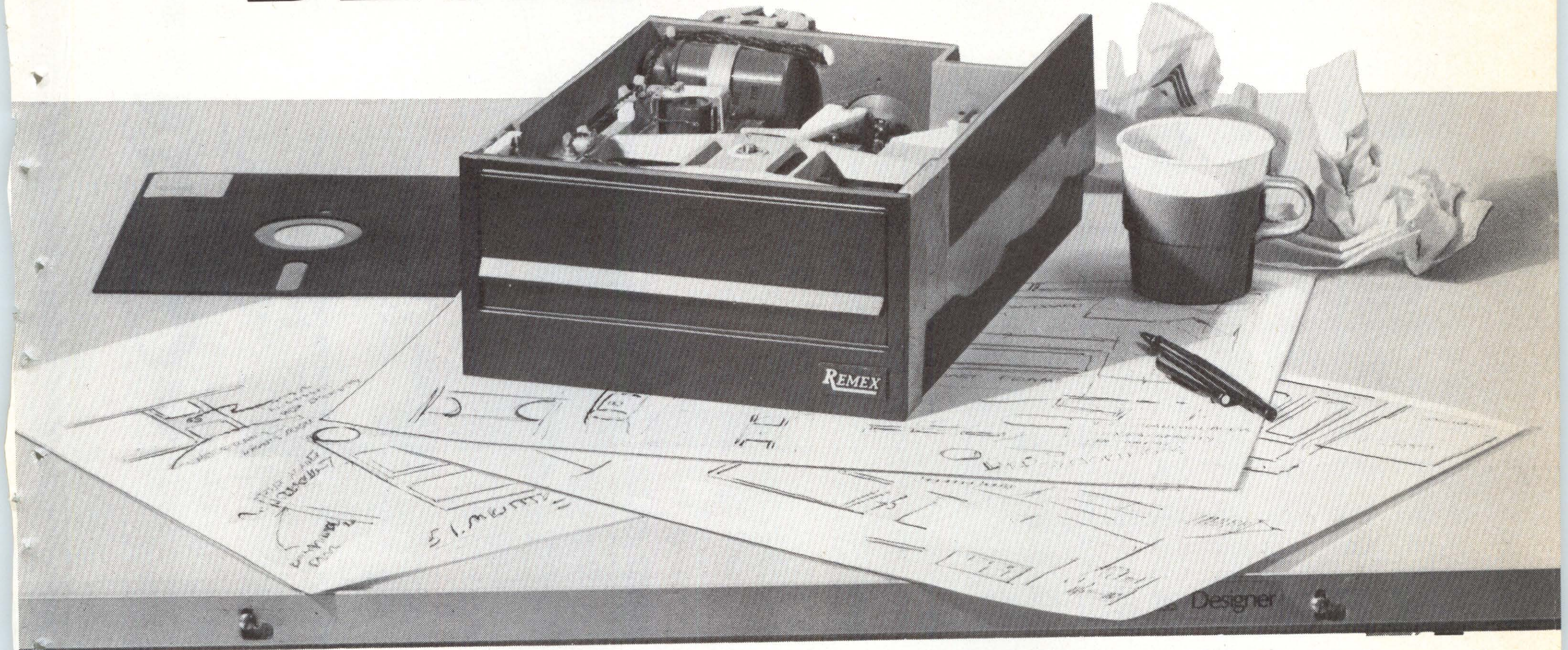
Random access, nonvolatile, destructive-readout ferrite core main memory is shared by the processors. Capacity is 65K 36-bit words, with each storage word made up of 32 bits of data, two store protect bits, and two parity bits. Although all 65K act as one memory, 41K words are physically located in the CPU box and 24K are in the IOP box. A lower cost alternative main memory incorporating volatile monolithic semiconductor storage is also available for use in shuttle computers allocated for ground installation in crew trainers.

Fixed-point data representation is binary, 2's complement, fractional. A halfword consists of 15 bits of data



Functional block diagram of one of five general-purpose computers to be used in space shuttle orbiter computer complex. CPU and IOP share 65K-word common main memory which is separated for packaging convenience. IOP consists of 24 independent processors which provide separate control over each of 24 serial data buses to interface shuttle subsystems. A twenty-fifth processor, the master sequence controller, controls operation of the other 24

MEET YOUR TOUGHEST DESIGN CRITERIA



MEET THE REMEX FLOPPY DISK DRIVE

No compromise required. There is one floppy disk drive with the design flexibility to meet all your systems requirements. The REMEX RFD7400.

IBM compatibility? Remex has it. Complete media and data interchange with 3740 Series systems. Guaranteed by Remex because the RFD7400 meets every one of the 3740 floppy disk specifications. We test for them!

Standard media? The RFD7400 provides a unique write enable option that gives fool proof operation on any standard IBM media. No need to pay a premium for specially prepared media. Select from any available source.

Fail safe design features? Our floppy disk drive has Track "00" and track "76" sensing. A unique feature which prevents machine damage and loss of data at *both* ends of diskette media.

Long life? How about 15,000 hours? The RFD7400 construction provides years of reliable operation with only 12 grams of head pressure, utilizing a tungsten-carbide ball bearing stylus. The result; 50% longer life than competitive units.

Extra capacity? You bet! Up to 3.2 megabits with our special hard sectoring and data recording options. And we use standard media too.

Random average access time? The RFD7400 is more than 30% faster than competition. Think of what this can do for your throughput.

Special configurations? The RFD-7400 can be custom designed to fit almost any application. Test us by sending your design headache to our Applications Engineering Manager. Better still, call us direct and order your evaluation unit for immediate delivery. Chances are that our standard unit already meets your requirements.

Write, Remex, a Unit of Ex-Cell-O Corporation, 1733 Alton Street, P.O. Box 11926, Santa Ana, California 92711 or call (714) 557-6860.

We work with you.

REMEX

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CIRCLE 25 ON INQUIRY CARD

plus sign; a full word is 31 bits plus sign. Floating-point data formats are 32 and 64 bits long, differing only in fraction size. The 32-bit length provides sine, 7-bit signal exponent, and 24-bit fraction; the 64-bit provides 56-bit fractions.

Design objectives for the computer complex include flexibility, reliability, low development risk, and low cost. Presentation of a paper on "Shuttle Computer Complex" explaining how these goals are being met was made by A. E. Cooper (speaker) and W. T. Chow of International Business Corp's Federal Systems Div in Owego, NY.

Microcomputer Profile Controller

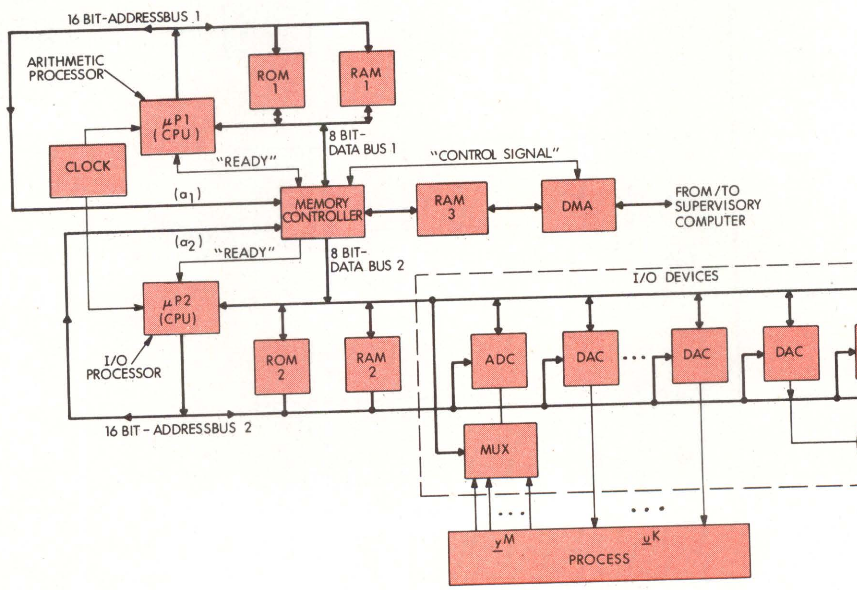
Profile or distribution control in distributed parameter processes is one of many application areas where microcomputers can advance the implementation of well known but rarely applied multivariable control concepts. A double-processor system with RAMs and ROMs and specified software can provide a flexible and adaptable profile controller. Aspects of the hardware and software design were reported in "The Design of a Microcomputer Controller for Distributed Parameter Systems" by G. Schmidt (speaker) and B. Posch of the Institut für MeB- und Regelungstechnik, Technische Universität München, Federal Republic of Germany.

A hardware concept for a special-purpose profile controller requires careful processing of algorithms as well as handling of measurement input and control output data. In a solution featuring a double-processor concept, one microprocessor is dedicated to the execution of profile control algorithms, including signal analysis and synthesis, while the other acts as an I/O processor. Basic functions are control of multiplexers and converters for measurement and control signals, signal conditioning, and control of a "quick-look" display for the desired and actual profiles.

Each processor functions with a small RAM and ROM or programmable ROM (p/ROM) as program storage devices. Interfacing from both processors to a supervisory process computer is accomplished by direct memory access to and from a third RAM, under supervision of a memory controller. A clock generator which serves both processors is used as a reference for the time basis of the profile controller programs. Functions of the controller can be adapted to various data processing control concepts and processes by changing data and/or replacing parts of the read-only storage.

Software must be organized such that it permits adaptation to a variety of processes. Principal mathematical operations must be programmed in separate modules: preparation (a number of routines executed at the supervisory process computer level) and executive and application (in modules for the two microprocessors). The first will be mostly in higher level language; the second will be made up of I/O, analyzer, algorithm, and synthesizer routines.

The authors feel that dedicated profile controllers are realizable from applications of microprocessor technology. Their investigations into a suitable hardware configuration and accompanying software show that such a controller can be adapted to various control concepts and measurement and control device patterns.



Developmental profile controller using double-processor concept. Each microprocessor has its own RAM stack and either ROM or p/ROM for program storage. DMA provides access to the supervisory computer through a memory controller that accesses a third RAM

(*Continued on p 50*)

Currently, functions of a profile controller with six non-interacting controller channels and up to 20 measurement inputs and control outputs were tested with an analog plant model.

Vocal Input Shows Promise for Machine Control

Although development of automatic speech recognition techniques is progressing, much more must be accomplished in order to achieve adequate recognition of connected sentences. Isolated words from limited vocabularies and highly syntax-constrained sentences can now be recognized, but further work is needed in connected-speech recognition, including segmentation of the speech wave, labeling, and syntactic analysis.

Man-machine communication by vocal input appears very promising, according to Jean-Paul Haton, Laboratoire d'Electricité et d'Automatique, University of Nancy, France. In a paper on "Automatic Speech Recognition in Oral Control of Machines" he described the application of a real-time isolated word-recognition system using syntactic constraints in numerical control of a machine tool.

This application uses a spectrum analysis technique to reduce the information rate of speech to a reasonable rate of 2400 bits/s. A word spoken into the microphone is represented by a pattern made up of a set of 24 component vectors (resulting from processing by a spectrum analyzer consisting of 24 bandpass filters covering the 110- to 7000-Hz range). Since each word must be separated from the next by at least 300 ms, sentences are made up of sequences of isolated words.

Recognition of an incoming word consists of matching it with reference vocabulary patterns. A single template is used for each word. Time-normalization of patterns is necessary because of the variations of time durations that might occur among several users pronouncing the same word. Nonlinear normalization used is based on a dynamic programming procedure which permits similar parts of two patterns to be matched by automatically adjusting differences in time duration.

The speech recognizer is based on a Nova 2/10 minicomputer with 16K words of core memory. Other components in the voice command system are a tape recorder, spectrum analyzer, paper-tape reader/punch, teletypewriter, and CRT display. Words are pronounced without special precautions in a noisy room to imitate an industrial environment. With a 40-word vocabulary the rate of correct recognition for one trained speaker is about 98%, with a computation time of less than 0.5 s. With several speakers the results decrease rapidly since neither frequency normalization nor special training processes are used.

Presently attainable performances of 95 to 99% recognition accuracy for tens up to 100 words, without use of syntactic constraints, are misleading, since only one error in direct control of a machine can cause dramatic damage. M. Haton predicts, however, that refinement of techniques as well as syntactic analysis in sentence recognition will improve accuracies.

Proceedings

All of the IFAC 75 papers abstracted here will be published in Vol IV of the Conference Proceedings: "Computers, Space Components, and Education." Hardbound copies of this and other volumes are available for $35 each from Instrument Society of America, 400 Stanwix St, Pittsburgh, PA 15222, or from John Wiley & Sons, Ltd, Baffins Lane, Sussex PO191UD, England.

Binary Signals Used in Multiplex Transmission of Analog Data

In one method devised for the multiplex transmission of analog data, binary signals in the 10-Hz to 100-kHz range are put to use. Frequency chosen depends on system parameters such as number of channels and sample rate required. In a circuit for such data transmission (Fig. 1), conceived by B. T. J. Holman of Philips Research Laboratories, Eindhoven, The Netherlands, the first pulse of input pulse train V_{in} brings all monostable multivibrators m_i ($i = 1, 2, \ldots$) from the "0" to the "1"

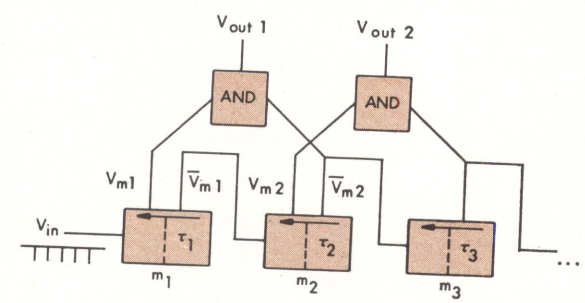


Fig. 1 Pulse pair detection circuit. $m_1, \ldots$ are non-retriggerable monostable multivibrators with fixed time constants $\tau_1, \ldots$

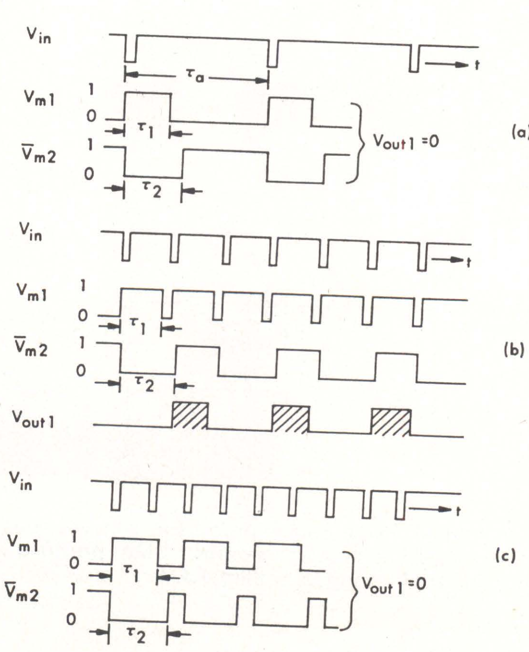


Fig. 2 Waveforms of Fig. 1. τ_a is time interval of succeeding input pulses. If $\tau_i < \tau_a < \tau_{i+1}$, an output signal is generated

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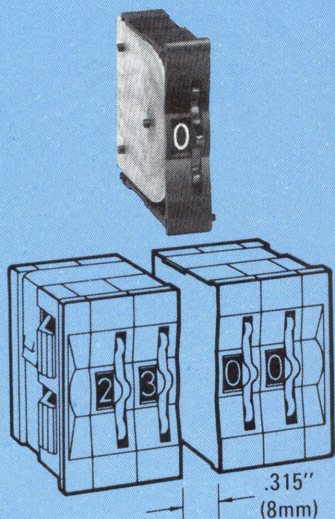

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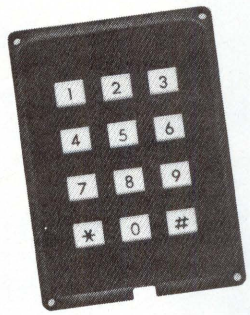

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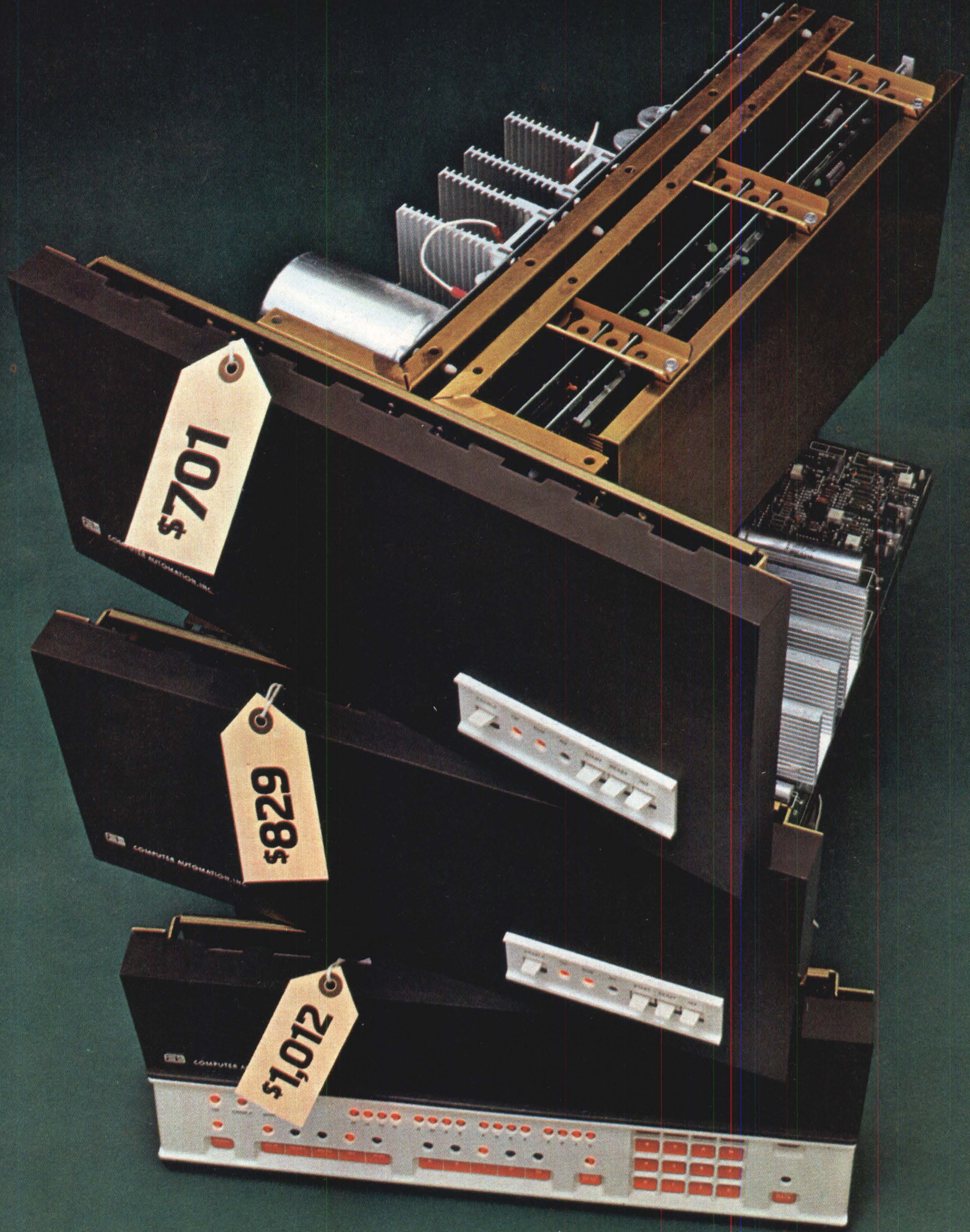

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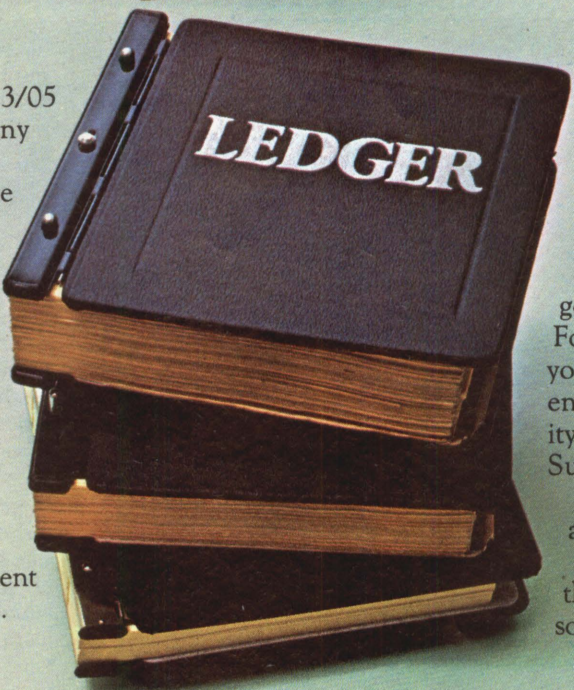

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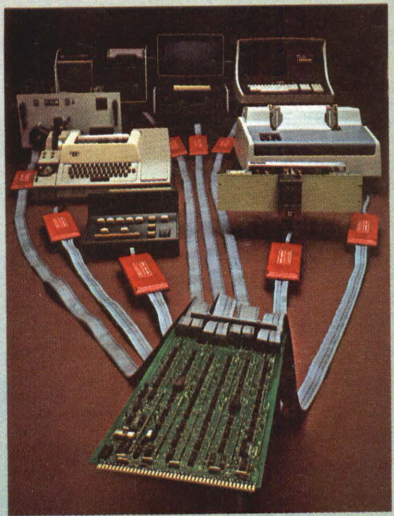

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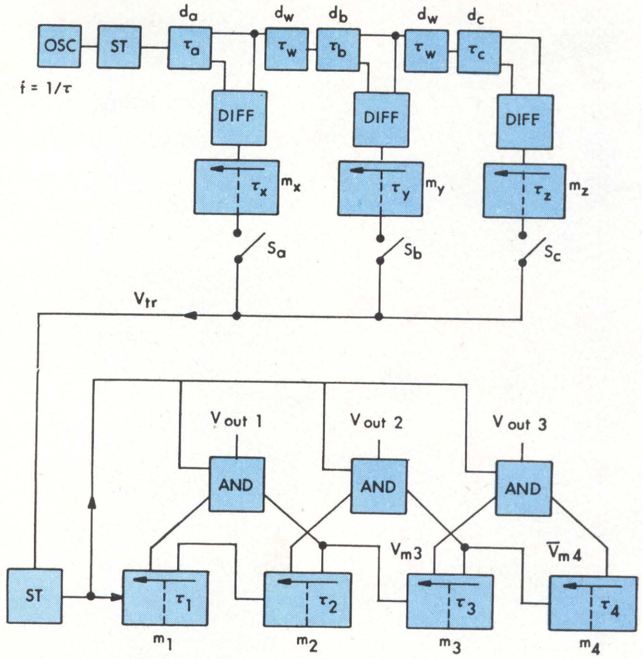

Fig. 3 Block diagram of transmission circuit with three channels. d_a, d_b, d_c, d_w, are delay circuits; m_x, m_y, m_z are monostable multivibrators with adjustable time constants τ_x, τ_y, τ_z representing the analog value of information to be transmitted; V_{tr} is transmission signal

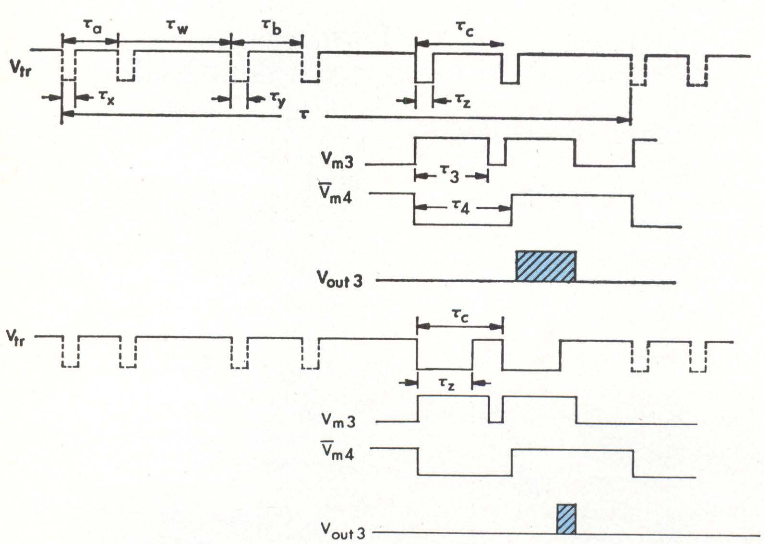

Fig. 4 Waveforms of Fig. 3; channel z operative. τ is cycle time of sets of pulse pairs, ie, pulse repetition time of the oscillator in Fig. 3. Full waveforms of V_{tr} indicates operative channel; dotted waveforms of V_{tr} are other channels. According to Figs. 2(a) and 2(b), output signal $V_{out\,3}$ is generated (cycle time τ). Width of $V_{out\,3}$ depends on the value given to τ_z

state. Each returns to the "0" state after a period equal to its individual time constant, τ_i. These time constants must fulfill condition $\tau_i < \tau_i + 1$ for all values of i; ie, they increase monotonously with i. If the second pulse in the pulse train comes at time τ_a after the first pulse, all multivibrators with a time constant smaller than τ_a are back in the "0" position, and will be returned to the "1" position again by that second pulse. Multivibrators having a time constant larger than τ_a are still in the "1" position, and thus they are not affected by the second pulse.

AND gates in the circuit are so connected that a signal, $V_{out\,i}$, is generated only if multivibrator m_i is in the "1" and multivibrator m_{i+1} in the 0" state. Figs. 2(a), (b), and (c) show that this will happen when their time constants obey the relation $\tau_i < \tau_a < \tau_{i+1}$. The circuit can therefore be said to be sensitive to pulse pairs, and time τ_a between the leading edges of the two pulses of pair $\tau_i < \tau_a < \tau_n$ determines which output is activated. If, after a pulse pair with τ_a, the delay is long enough for all multivibrators to return to the "0" state, another pulse pair can be given with spacing τ_b to activate another output.

The circuit has been extended so that each output can be controlled by the width of the individual pulses of the corresponding pulse pair. Width of each of the pulses is varied; and the width represents the analog value of the information to be transmitted. If the transmitted input signal, V_{tr}, is now added to the AND gate, the output signal shows a content that depends on this pulse width.

Fig. 3 is a diagram of a sending and receiving circuit for a 3-channel multiplex, pulsewidth-modulated transmission system. An oscillator pulse with cycle time τ, squared by a Schmitt trigger, ST, is used to compose the transmission signal, V_{tr}, with the aid of delay circuits d_a, d_w, . . . (preferably monostable multivibrators) with fixed delays τ_a, τ_w, τ_b, . . . , differentiating circuits and monostable multivibrators (m_x, . . .) with variable pulsewidths τ_x, ... In Fig. 4 these widths represent the analog values of the information to be transmitted. Switches S_a, S_b, . . . determine whether or not information is transmitted. Output signal $V_{out\,3}$ is shown for the case where only channel z is in operation. All channels can be used simultaneously.

Possible applications are in industrial remote control and traffic control. However, the results described refer to laboratory experiments and do not necessarily imply a follow-up in production or marketing. □

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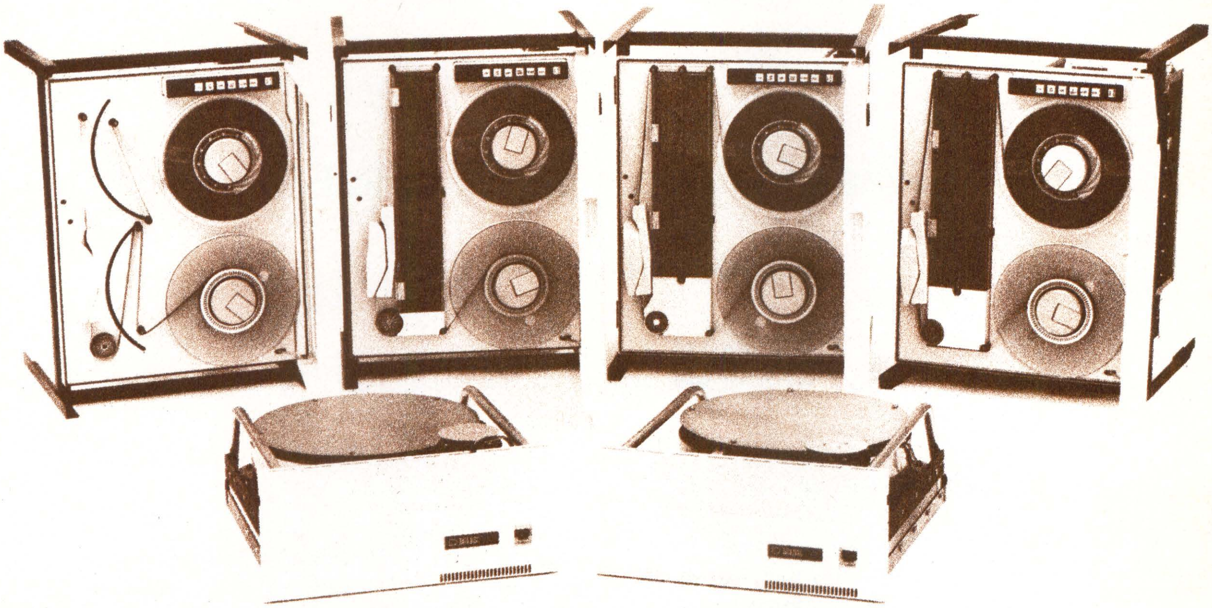

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The Role of Microcomputers in Robotics

K. Goksel* and E. A. Parrish, Jr

University of Virginia
Electrical Engineering Department
Charlottesville, Virginia

Having found a place in dedicated applications as diverse as industrial control and electronic coin-operated games, it should not be surprising to see microcomputers also playing active roles in robotics. Their slow speeds (relative to state-of-the-art minicomputers) are not deterrents since any processing delays would be small compared to other time constraints in the system hardware. In addition, their low cost and ability to function reliably in adverse industrial environments are important incentives.

The basic commercially-available industrial robot is a machine that is sequentially driven to points whose coordinates are stored in memory. More sophisticated robots are programmed by "teaching," where a skilled worker leads the machine through the task while positions are stored in memory. These robots are equipped with very few low-level sensors.

Only the robots in research laboratories and institutes use sensors of considerable complexity and have a computer that enables them to interpret the sensory information and make decisions accordingly. Commercial robots of the next decade, however, are expected to be equipped with vision, including a ranging device, and a set of tactile (force, torque) sensors. They will be able to modify their tasks by making decisions based on the information collected from the environment.

In most complex systems, task and trajectory planning and execution as well as sensory information interpretation are handled by a central computer. The low cost of microcomputers makes them very attractive for decentralizing these functions. In the system described here to illustrate the role of the microcomputer in the robot of the future, a supervisory minicomputer handles task and trajectory planning while a localized microcomputer attends to the control of the robot while simultaneously interpreting sensor functions. A suggested application for a feasible present-day commercial robot has a microcomputer acting as a standalone controller for a "programmable by teaching" robot.

Multiprocessor System

One system under development at the University of Virginia uses a Hewlett-Packard 2100A minicomputer with 16-bit word length as the central computer and an Intel MCS-4 microcomputer as a control processor. An I/O channel for the minicomputer consists of a dual 16-bit buffer, a control bit which serves as a request line to the microcomputer, and a flag bit which is set by the microcomputer to interrupt the minicomputer to acknowledge the completion of an operation. The microcomputer is made up of an Intel 4004 microprocessor, 1K-word x 8-bit p/ROM, 320-word x 4-bit RAM, and I/O buffers.

Data describing the task are transferred to the microcomputer from the minicomputer as a sequence of macrocommands along with arm-joint positions and constraints on force levels and trajectories. After transferring these data, the minicomputer continues processing the central routines. The microcomputer interprets the data, executes the macrocommands by utilizing the information fed back from position potentiometers and sensors, and interrupts the minicomputer when the task is completed. At this time, the microcomputer transfers the final joint positions and the status of the sensors to the minicomputer. When not executing a task, the microcomputer maintains the joints in position, continuously scanning the joint potentiometers.

The manipulator (Fig. 1) is a general-purpose industrial arm with one translational and five rotary joints. All joints are hydraulically powered, but the prime mover is pneumatic. The arm is equipped with a gripping mechanism or hand which consists of parallel gripping fingers, a palm that moves along the surface of the fingers, and clutching prongs to grasp irregularly-shaped objects. An extension plunger in one of the fingers can be used to press pushbuttons. Tactile information is derived from touch sensors placed on the

*Dr Goksel is now associated with M B Associates, San Ramon, Calif.

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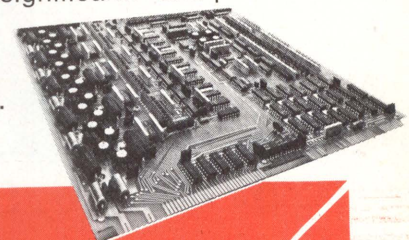

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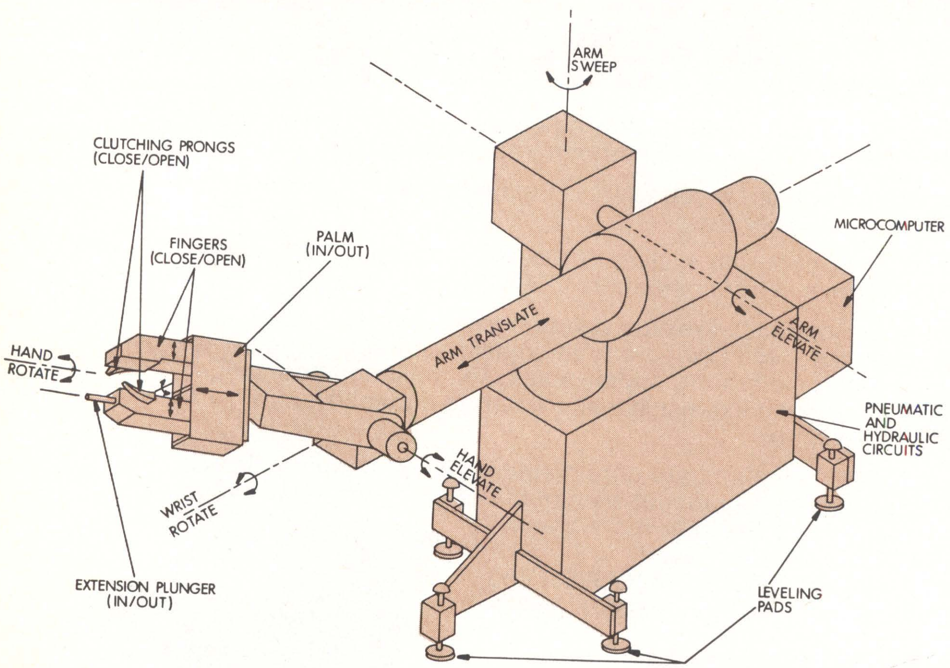

Fig. 1 Industrial manipulator equipped with one translational and five rotary joints. Hand consists of parallel gripping fingers, palm, clutching prongs, and extension plunger. Tactile information is derived from touch sensors on fingers and palm. Microcomputer receives task identification from a supervisory minicomputer (Reprinted with permission from Ref. 1)

inner faces of the fingers, palm, tips of fingers, and outer surfaces of the fingers. The touch sensors on the inner face of one of the fingers are arranged in a 2 x 4 array to provide information for rudimentary pattern recognition. Slip sensors located on the inner faces of each finger indicate slippage of a grasped object. Position feedback is provided by direct-coupled, continuous film potentiometers on the joints.

Manipulator joints are controlled in a bang-bang dual-speed mode (fast traverse and slow close-in). As indicated in Fig. 2, data from position potentiometers are multiplexed to a 12-bit A-D converter through an

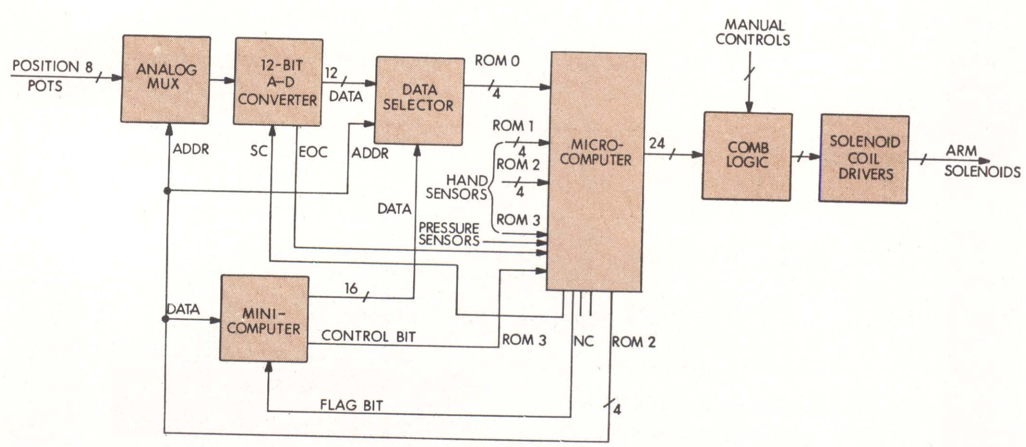

Fig. 2 System data flow diagram showing arrangement of minicomputer, microcomputer, and associated interface. Manipulator joint positions are scanned by analog multiplexer, analog-to-digital converter, and data selector (Reprinted with permission from Ref. 1)

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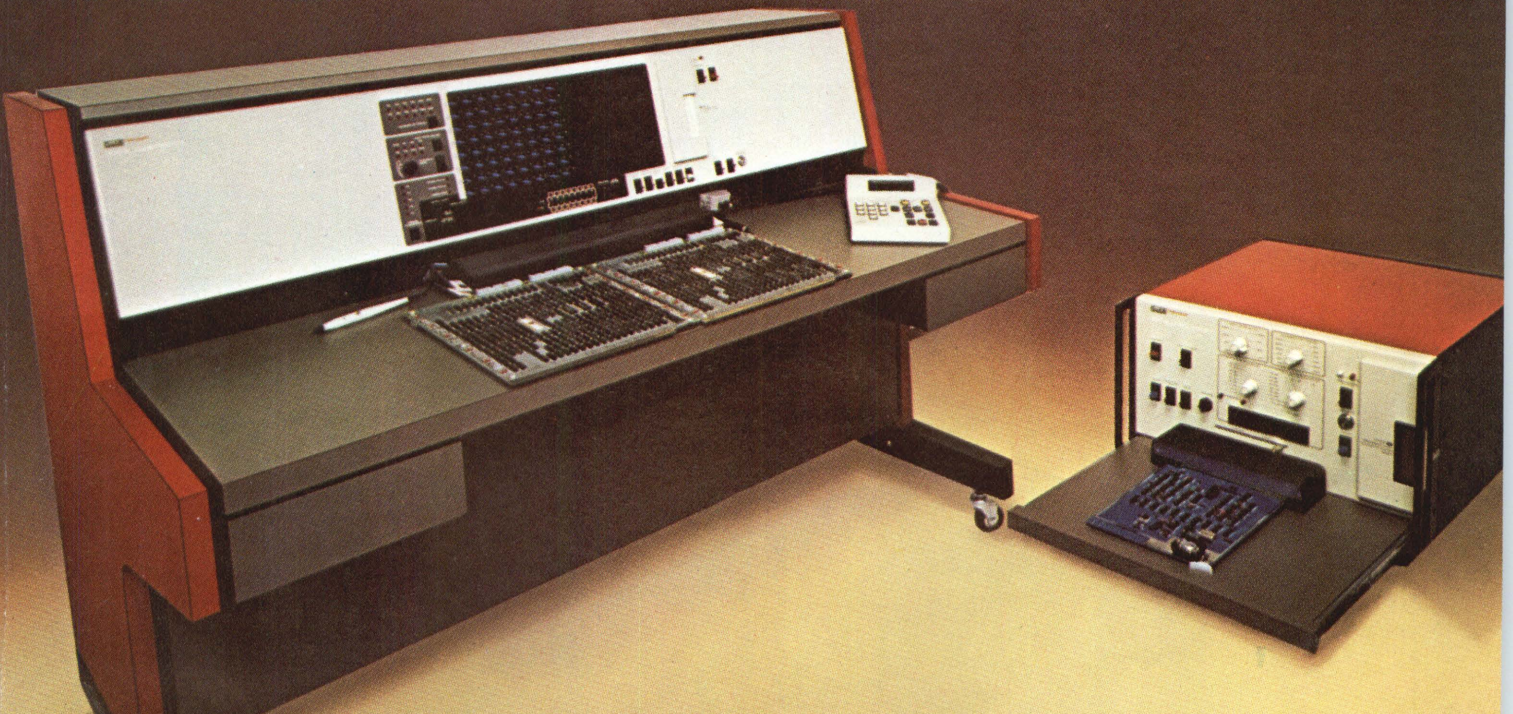

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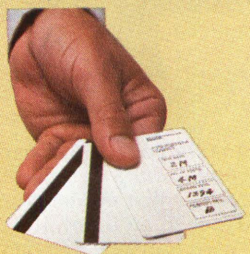

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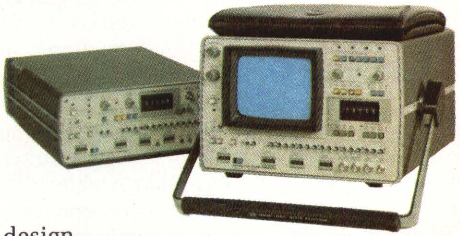

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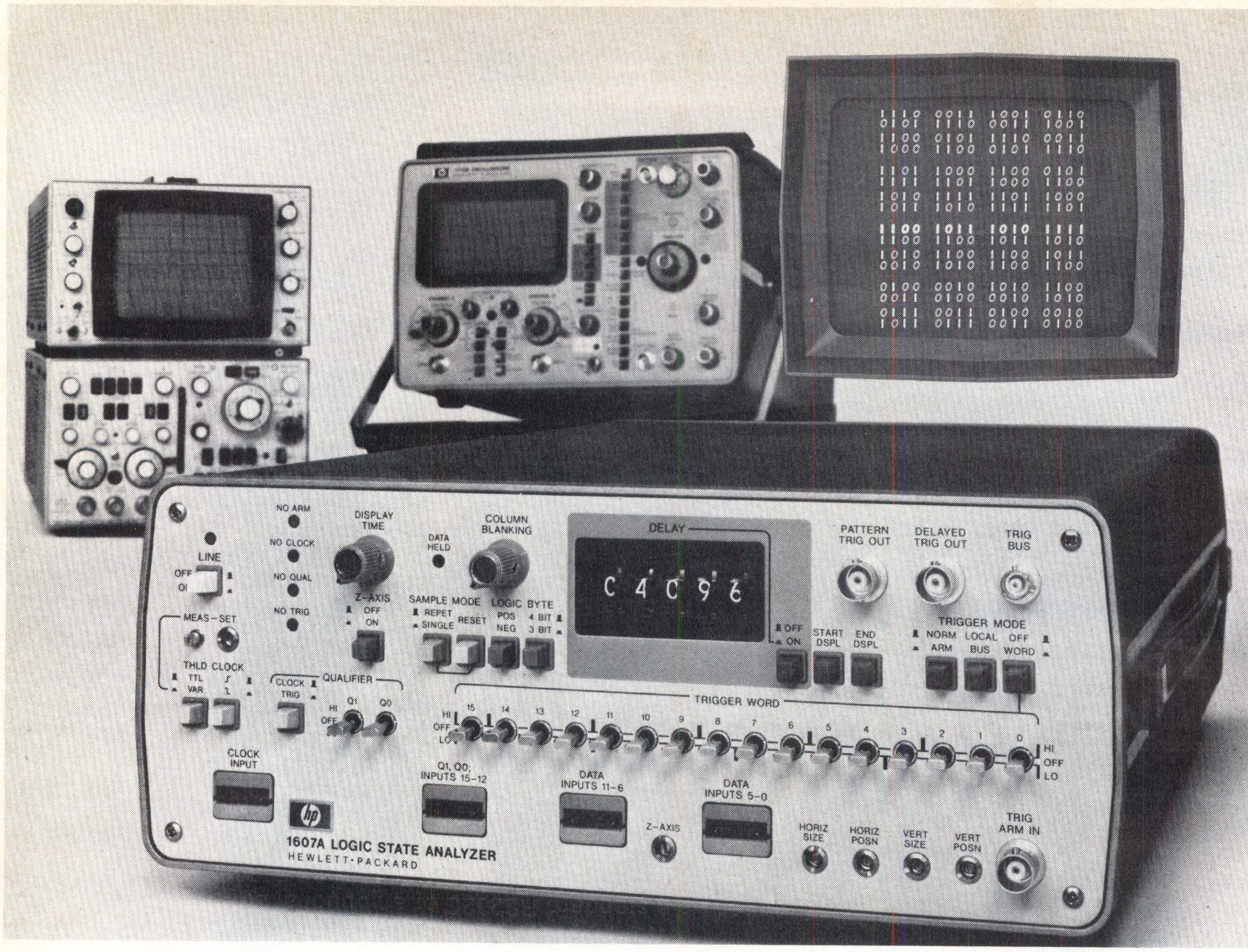

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analog multiplexer that is made up of two 4-channel chips. The 12-bit digital position is multiplexed to a 4-bit input port by a data selector composed of four multiplexer chips. Four of the data selector's channels are used to multiplex the 16-bit data from the minicomputer to the 4-bit input port.

The microcomputer receives data from the minicomputer and position potentiometers on the arm, and monitors hand sensors, pressure sensors, the control bit from the minicomputer, and the End-of-Conversion signal from the A-D converter. Data to the minicomputer and addresses to the analog multiplexer and data selector are sent on a 4-bit bus connected to one output port. The Start Conversion command to the A-D converter and flag bit to the minicomputer are sent through two output lines. Valve solenoid coils are controlled by 24 output lines from the microcomputer through optically coupled photo-SCRs. Solenoid coil driver boards are isolated from the rest of the hardware by a metal card grounded to the card cage.

Software

The supervisory minicomputer handles scene analysis and task and trajectory planning routines (not discussed here since they are beyond the scope of this article). After planning the task, the minicomputer interrupts the microcomputer (by setting the control bit) to transfer the data that describes the task. The minicomputer specifies a task by sending a group of 16-bit command words to the microcomputer. Each such task description consists of a list of macrocommands, made

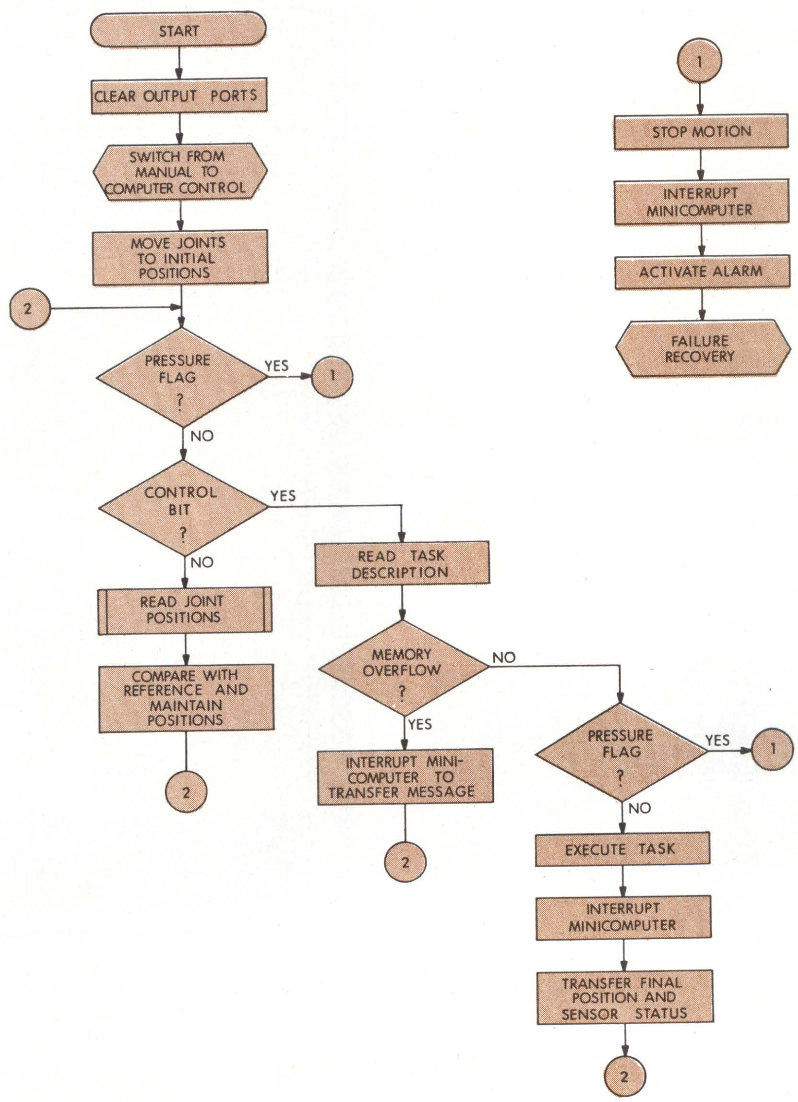

Fig. 3 Microcomputer control routine. Microcomputer interprets task description, executes macrocommands utilizing position and sensory feedback, and returns final position and sensor status to the minicomputer

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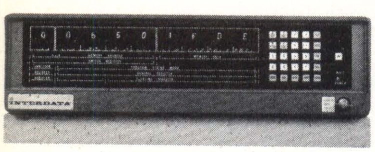

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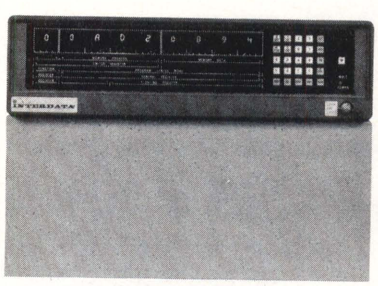

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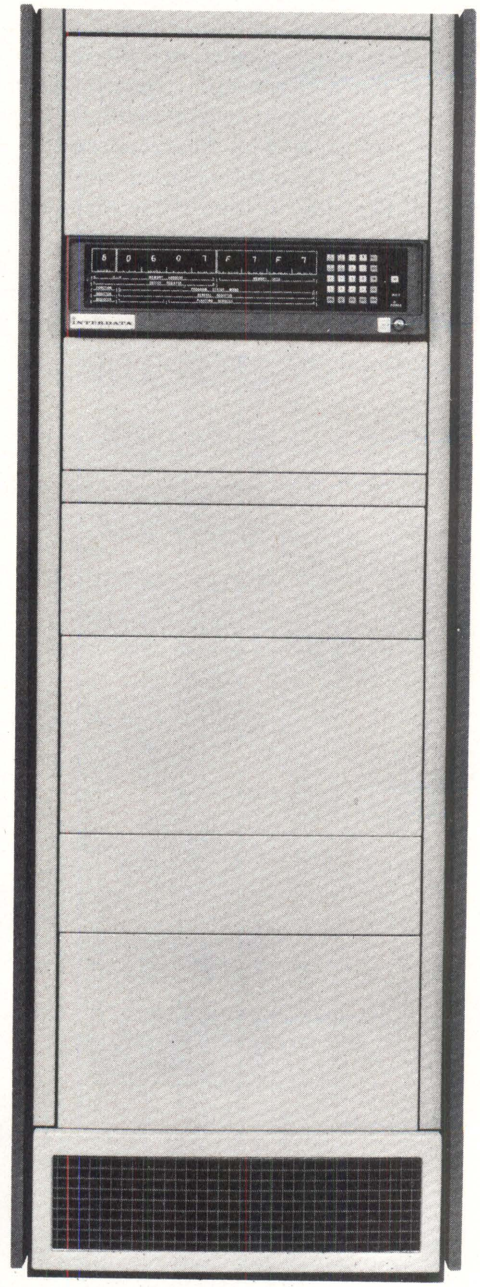

Interdata's 8/32 Megamini is the industry's most powerful 32-bit minicomputer. It is an unequalled combination of power, flexibility and reliability compactly packaged.

up of 4-bit bytes, along with data for joint positions and constraints on force levels and trajectories.

A maximum of three macrocommands may be listed in one 16-bit word since the first 4-bit byte (most significant byte) of the word acts as an identifier for the rest of the word to distinguish between macrocommands and different types of data. Macrocommands are executed in the order sent in the data transfer. A joint position is specified in 12 bits preceded by the joint-position data identifier.

Macrocommands are instructions to move the specified joints of the arm (see Table). Their use enables the user, who programs the supervisory routines, to avoid involvement with the details of the arm.

Eleven different force levels can be applied by the hand. The force level data word uses the first three bytes of the 16-bit word: the identifier, followed by the minimum and maximum force levels in the next two bytes.

Constraints can be placed on the relative positions of the joints throughout a trajectory using a constraint data word made up of two 16-bit words. The task description is terminated by an Execute command, which consists of a 16-bit word containing the associated tag. Only the most significant 4-bit byte of this word is read by the microcomputer. The minicomputer continues processing central routines after transferring the task description.

In the microcomputer control routine (Fig. 3), manual reset starts the program. Output ports are cleared by software and the arm is switched from manual to computer control. Joints are then driven to a set of predetermined reference positions. The microcomputer maintains these joint positions within a specified tolerance by sampling joint potentiometer readings, comparing them with the reference positions, and making the necessary corrections. Fig. 4 illustrates the joint-position reading routine. The control bit and the pressure sensor

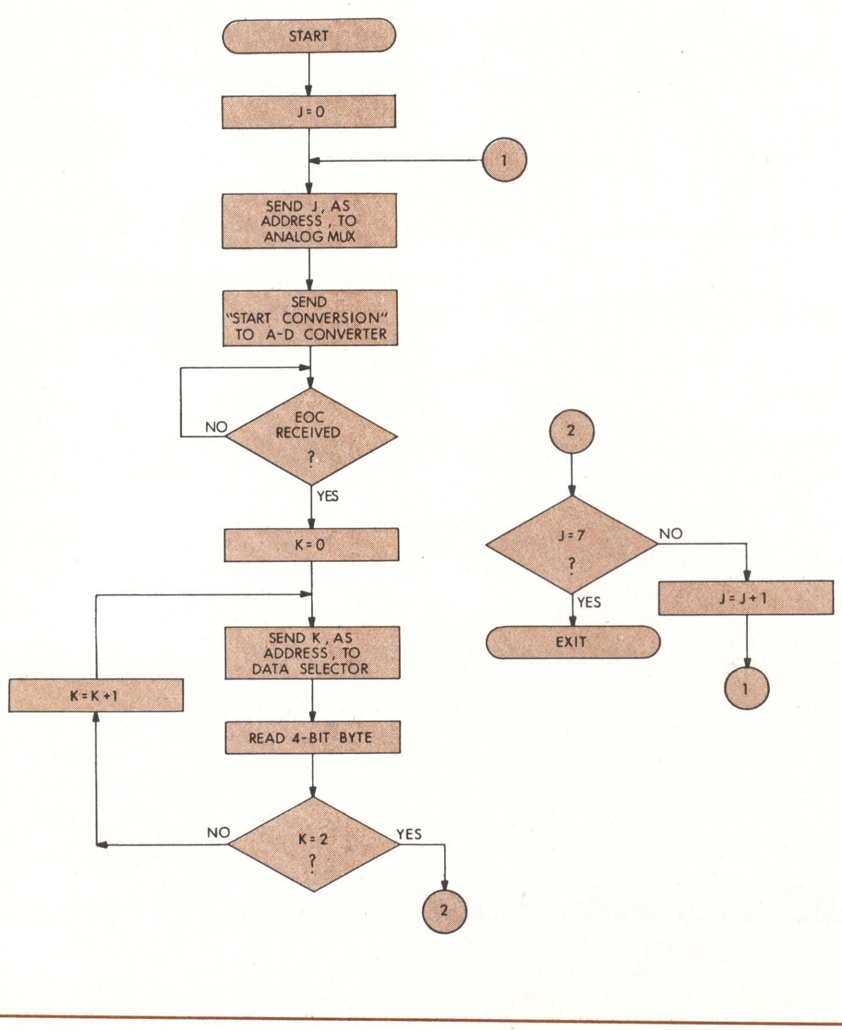

Fig. 4 Joint position reading routine. Microcomputer scans joint positions through analog multiplexer, analog-to-digital converter, and data selector

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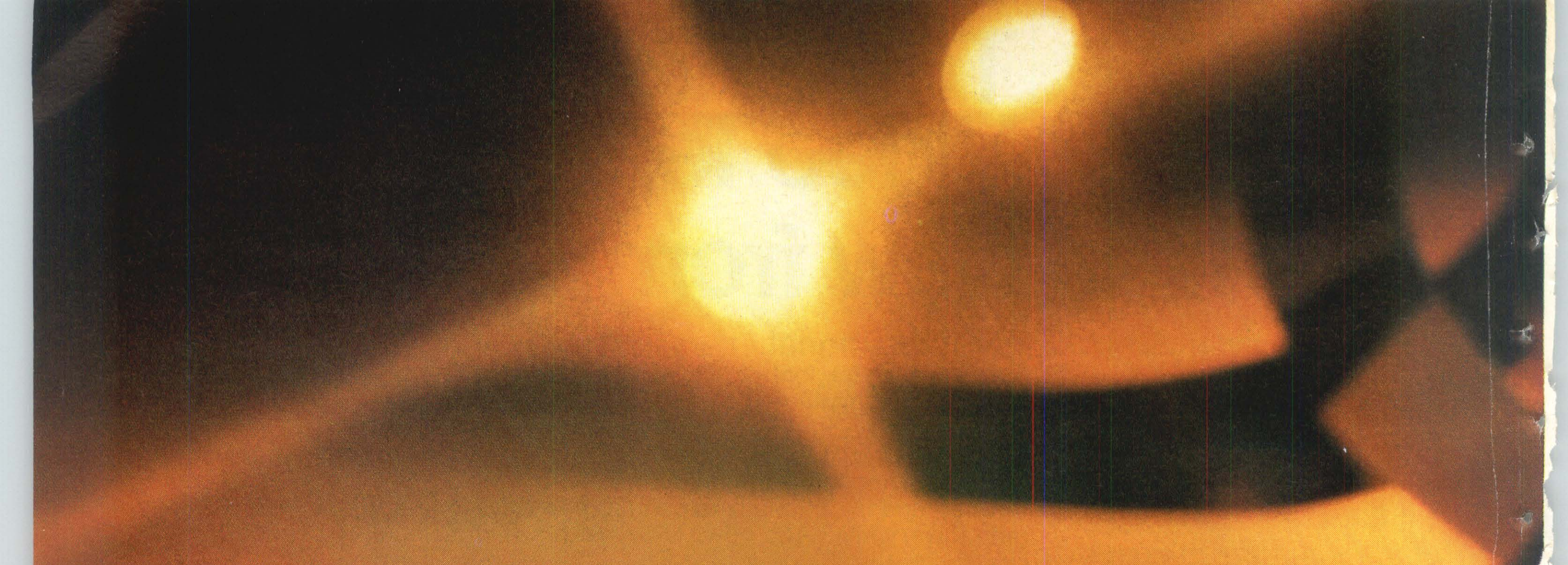

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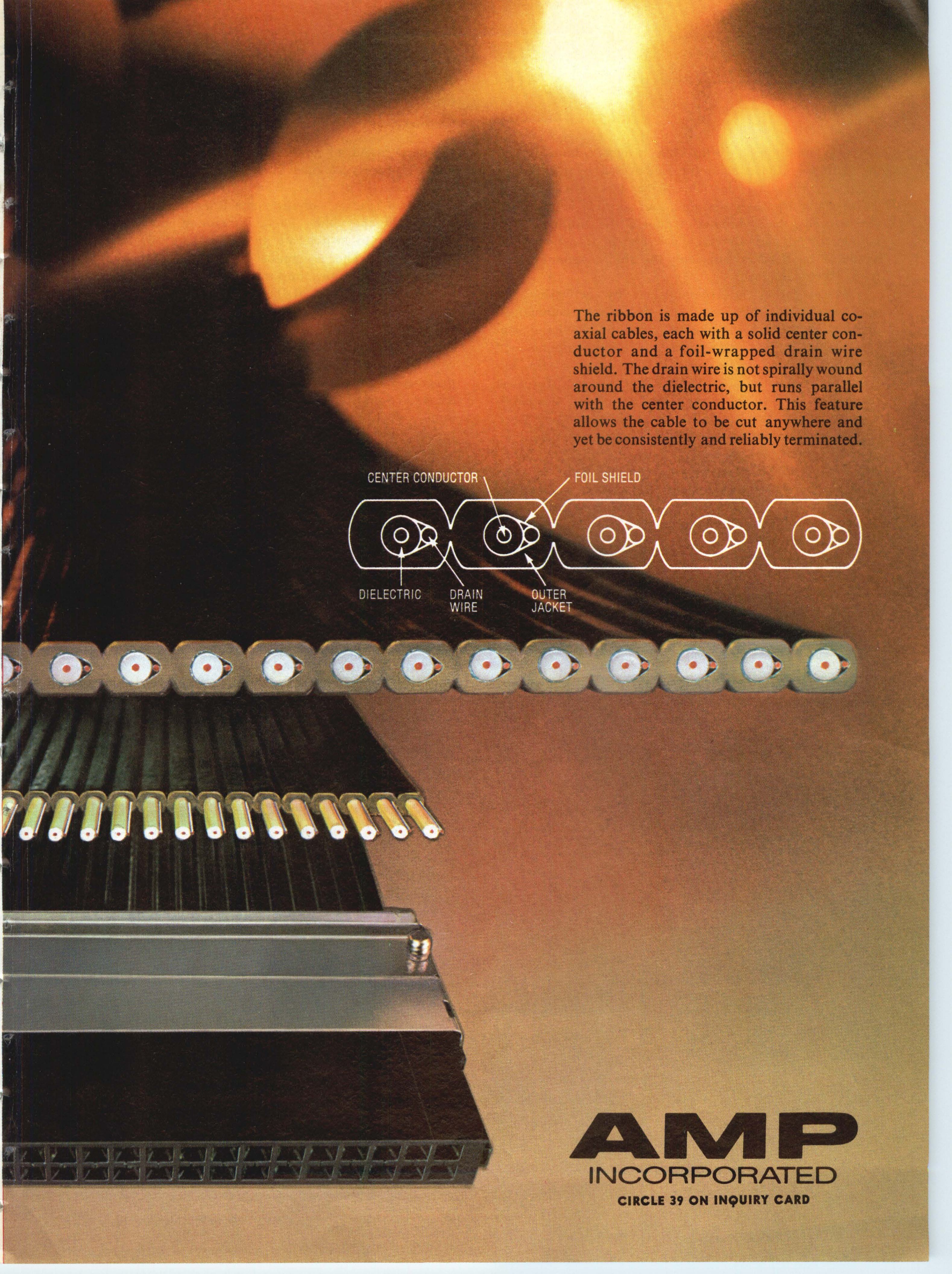

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are also monitored within this program loop. When the setting of the control bit is detected by the microcomputer, the data describing the task are received. These data are then decoded and stored. If the data size exceeds the available memory, the minicomputer is interrupted and an error message is transferred; if available memory is sufficient, the microcomputer goes on to execute the task.

Task execution is accomplished by activating the appropriate control lines for the given commands, utilizing tactile information provided by the hand sensors. When holding an object, the microcomputer will raise the applied force by one level when a slip flag is received. If the slip flag is not cleared, force is increased one level at a time (not to exceed the maximum) until it is cleared. A delay is allowed between slip-sensor samples to permit the hand to respond.

Moving to a new position is accomplished by replacing the reference positions in memory with the new joint positions and branching to the position-maintaining routine. When the task is completed, the microcomputer interrupts the minicomputer and transfers the final joint positions and sensor status. The microcomputer maintains this position until a new task request is received.

The pressure sensor is queried throughout the process. Loss of pressure in the arm hydraulics or pneumatics sets the flag, causing the microcomputer to stop motion, interrupt the minicomputer, and activate both visible and audible alarms.

Less than 1K x 8 bits of p/ROM storage is required by the program. RAM storage of 320 words x 4 bits has been found adequate for most tasks. Position error due to processing time is small when compared with other sources of error. The longest time interval between two readings of the same joint position is under 3 ms. On the other hand, maximum times for the photo-SCRs to switch off and a solenoid to drop are 8 ms each. The dynamics of the hydraulics would raise the total time constant to a worst-case figure of 30 ms. A low speed of 0.3 in./s would cause a worst-case error of less than 0.01 in.

Macrocommand Set

Mnemonic	Code	Command Word
E	0000	End list
P1	0001	Position all specified joints simultaneously
P2	0010	Position all specified joints in specified order
P3	0101	Position all specified joints simultaneously at slow speed
P4	0110	Position all specified joints in specified order at slow speed
PT	1100	Position hand with touch feedback
PH	1110	Position hand followed by hold
PG	1111	Position hand followed by grasp
HH	1000	Hold
GG	1001	Grasp
RR	0111	Release
TE	1010	Thumb extend
TR	1011	Thumb retract

Microcomputer as a Standalone Controller

Not only are microcomputers functional in a multiprocessor control environment, they can also be used as standalone computers in some applications. An example would be a manipulator which is "taught" the task it is to perform.

A microcomputer controller can be used to sample and record positions into memory while a manipulator is lead through a task under manual control. The task would then be repeated by a program which causes the manipulator to track the stored positions. Position recording can be done either in a synchronous fashion, where the sampling frequency is preprogrammed, or asynchronously where the store command is given by the operator. Each position requires 24 x 4 bits of memory for storage for the manipulator discussed here. Hence, a task described by 1000 points would require 24 kilobytes of storage. However, this requirement may be reduced by using selective storing, ie, recording only the joint positions in which a change has occurred with respect to the previous position.

In "play-back" mode, when the manipulator is made to track the stored task, the microcomputer can again be used to many advantages. The task can be modified during execution according to information derived from the sensors.

An example for this application is an "inspection" situation where the parts manipulated by the hand are placed in different locations according to their size. Size of a part is derived from the opening of the fingers. A record of the measurements may be obtained, if desired, by listing them on a printer.

Programmable tracking accuracy can also be used during task execution. This feature would increase manipulator speed by imposing a low level accuracy requirement on intermediate points on the trajectory.

Finally, the microcomputer can be programmed to monitor the sensors and to indicate a failure in the system or the presence of a human being or an object at an unexpected location. Detection of any of these events would cause the microcomputer to terminate motion.

In another configuration, the minicomputer in the first system is replaced by a human operator and a teletypewriter. The operator types the task description using the same format employed with the minicomputer. The microcomputer executes the task and prints the final joint position and sensor status on the teletypewriter. This configuration has been found especially useful as an intermediate stage during the development of the multiprocessor system.

Conclusion

In the described system, which uses a microcomputer as a control processor for an industrial robot, parallelism in processing is achieved by allowing the minicomputer to handle central routines while the microcomputer attends arm motion. The system is general in the sense that it can be extended to different central computers, different industrial manipulators, and various microcomputers. Modularity in software and hardware improves the efficiency as well as the reliability of the system. Use of macrocommands simplifies central computer routines, relieving the user from the details of the manipulator control.

As an immediate application of a microcomputer in today's commercial robot as a "programmable by teaching" controller, it is suggested that the use of a microcomputer may provide data reduction by selective storing, programmable tracking accuracy, ability for the robot to modify the task during execution utilizing sensory feedback, and facilities for the implementation of safety features.

Several additional applications for microcomputers in robotics can be suggested. Using a microcomputer as a preprocessor for a TV camera, which provides vision for the robot, would control the associated fast interface that digitizes the picture and stores it in memory. It might then perform a data reduction, obtain a feature signature, and transfer this signature to the central computer.

A microcomputer also can be used as a tactile sensor processor, with sensors sampled through an analog multiplexer and an A-D converter. The microcomputer would then compare digitized sensor outputs with programmed thresholds and set the appropriate status lines to the control and central computers.

Additional areas where a microcomputer could be used include a voice-command interpreter and a laser ranging-device controller. In addition, for assembly tasks which usually require systems with multiple arms, a microcomputer locally controlling each arm would provide simultaneous motion of the arms.

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4. "Computer '75," *Electronic Design*, May 10, 1975, pp 32-95
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CIRCLE 42 ON INQUIRY CARD

In many cases instrumentation systems and similar test projects can be controlled by a calculator just as well as by a minicomputer, often at less cost; here are some of the tradeoffs involved

Programmable Calculators Control Data Acquisition Systems

Jerry Estes

Hewlett-Packard Company
Loveland, Colorado

For the past several years programmable calculators have been approaching those capabilities once solely in the minicomputer's domain. Today's calculators have sufficient memory capacity and language to displace minicomputers in most instrumentation systems. Technology has accelerated their capability to the point where they can do the same job as minicomputers—yet more people find them easy to understand, and use them because they need not wait for a computer programmer or for keypunch service.

When applying a programmable calculator in an instrumentation system, memory cycle time is seldom a limiting factor. Instead, speed restrictions are almost always imposed by digitizing of analog signals. Many physical parameters do not change fast enough to justify data rates exceeding 10,000 measurements per second, and most, such as temperature, require only a few readings per second.

Acquisition, storage, and manipulation of data are common to all engineering disciplines. The parameter of interest is usually not electrical, and must be converted, by a transducer, to an electrical signal. A broad spectrum of such transducers is available for converting physical parameters, such as acceleration, pressure, angular position, or velocity, to an electrical signal. If many measurements are necessary, the easiest course is first to convert them to analog voltages and then to digital form; alternatively, a nonelectrical quantity may be directly digitized.

Data acquisition systems are used in three basic areas: research and development laboratories, process industries, and factory production. In laboratories they monitor electrical and physical parameters of experimental systems. In process industries they monitor process parameters, calculate and predict trends, and occasionally control the process itself on the basis of these calculations. Finally, in factory production, they permit more complete testing of the factory's product in less time—for example, testing printed circuit boards for faulty, incorrect, or missing components.

Data acquisition is not necessarily complex. It can be as simple as a digital voltmeter and a printer, logging voltage measurements that represent other variables, such as pH or temperature. On the other extreme, it can involve data from multipoint transducers, periodically scanned under the control of a computer. The latter reduces data online and makes appropriate calculations to correlate data, test limits, and predict trends, such as the sulfur dioxide (SO_2) concentration in the thick juice when extracting sugar from sugar beets where the system can also control the process by modifying the SO_2 generating mechanism.

Gas Turbine Measurements

The steps required to instrument an experimental gas turbine offer an example of the use of a programmable calculator as the controller for data acquisition. At Chrysler Corporation's engineering center in Detroit, where a program for gas-turbine development is under way, researchers in the component test lab have increased the speed and sophistication of their data gathering and analysis by this means.

By nature, turbine and compressor component tests require large amounts of data to properly characterize their operation. These data, primarily temperature and pressure, may include up to 18,000 individual measurements during one test. Measurements are taken on 70 temperature channels and on 196 pressure channels using signal levels ranging from 10 mV to 16 V. From these measurements, the system calculates efficiency, slip factors, pressure ratio, and air flow; compensates for nonlinearities in the transducer; and records the results on a digital plotter and a paper-tape punch.

System Considerations

Any instrumentation system requires consideration of four areas: transducers, measurements, linearization, and programming.

Transducers develop usable electrical output signals in response to physical phenomena—specifically temperature and pressure, in the gas turbine project. The turbine requires temperature measurements in the range from 50 to 800°C, most easily measured with a thermocouple (a junction between two dissimilar metals, which creates a voltage related to its temperature). In thermocouples, sensing and transduction take place in the same element, which requires no external power.

Theoretically, three quantities are necessary in applying thermocouples. One is the voltage generated by a thermocouple at the point where the temperature is to be measured; a second is a reference voltage, generated by another thermocouple at a point of known temperature; and a third is the thermocouple characteristic, which describes the behavior of the junction as its temperature changes from the reference level toward the unknown.

In practice, the third quantity is assumed, because highly standardized commercial devices have precisely known characteristics. The second quantity, thermocouple response at a known temperature, can be obtained from the meter leads themselves, which form reference junctions where they are connected to those of the thermocouple at the unknown temperature. These connections, in general, involve different materials and can be maintained at a fixed temperature by immersion in an ice-water bath, or by otherwise refrigerating or heating them.

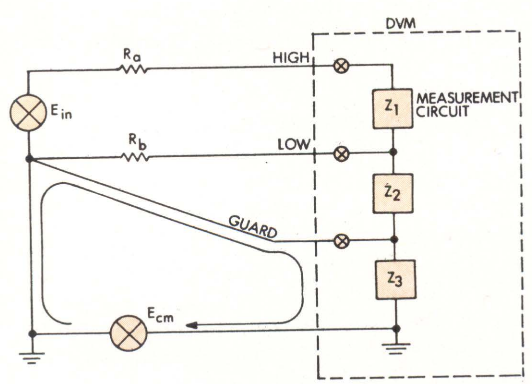

Fig. 1 Noise guard. Protection from worst effects of common-mode noise is obtained by shielding meter leads and circuits with a conductive guard grounded at the end opposite the meter. The guard shunts common-mode current (color) away from the meter

Pressure is measured through a mechanical multiplexer connecting one pressure transducer to many pressure lines. It avoids the expense of a pressure transducer for each data channel.

Measurement

At low levels, such as the approximately 50 $\mu V/°C$ developed by thermocouples, measurement accuracy is often limited by normal- and common-mode noise. Normal-mode noise appears between the two voltmeter inputs, superimposed on the desired signal. It can be minimized only by filtering.

Common-mode noise appears on both voltmeter inputs when meter and signal-source references are separate. In a perfectly balanced system, the appearance of common-mode noise will not create a problem; however, no system is perfectly balanced. Therefore, this form of noise is minimized by using a voltmeter guard—an electrostatic shield which surrounds input lines and measurement circuits and is connected to signal ground (Fig. 1). This connection shunts the common-mode current away from the measurement circuit. The meter's internal impedance to system ground, Z_3, is on the order of $10^7\ \Omega$, and the guard circuit's impedance is low—no more than 10 Ω. These two impedances form a voltage divider, with a ratio which is approximately equal to the common-mode rejection. For the impedances cited, rejection ratio is 120 dB.

When a system includes many channels of a single type of measurement—as 70 temperature channels in the case of the gas turbine project—some form of multiplexer must be included in the system to commutate the various channels to the digital voltmeter, regulated by the system controller. Thermocouple channels and multiplexer must impose little or no thermal offset—a positive or negative voltage added to that of the thermocouple, which could be interpreted as a temperature error. Another requirement is 3-wire switching, which is necessary to maintain guard continuity through the multiplexer. If a single multiplexer has insufficient capacity, two or more can often be used in tandem, connected to a common bus.[1] For example, the HP 3495A scanner provides forty 3-wire channels with low thermal offset.

Linearization

Many transducers are nonlinear. Although they may sometimes be assumed linear over a restricted range, nonlinearities must usually be taken into account over an extended range—for example, with tables or calibration curves, which may either be imprecise or use large memory spaces. In data acquisition systems, the calculator provides a powerful tool for linearization, correcting the measurement with a power-series polynomial that describes the thermocouple table. For example, a polynomial of degree 5 can describe a particular thermocouple to an accuracy of 1°C over its entire operating range. Execution time is saved by using the polynomial in its nested form, ie, the second expression following:

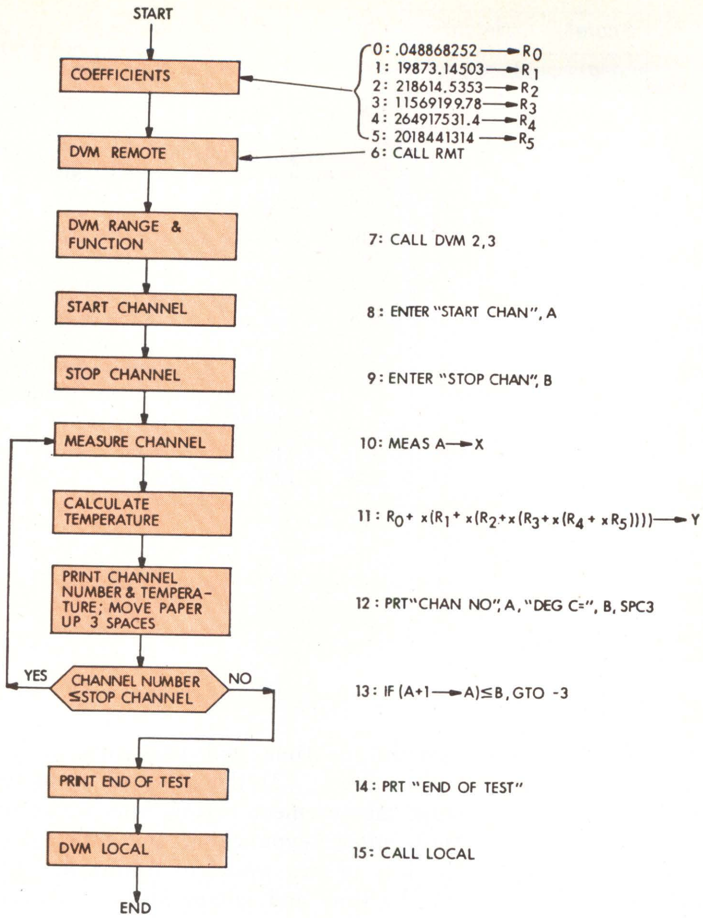

Fig. 2 Easy programming. Calculator is programmed from keyboard, which has a key for each function to be performed. Listing of instructions is matched to steps in the flowchart

$$T = a_0 + a_1x + a_2x^2 + a_3x^3 + a_4x^4 + a_5x^5$$
$$= a_0 + x(a_1 + x(a_2 + x(a_3 + x(a_4 + a_5x))))$$

This equation can be stored in the calculator's memory and used for many thermocouples of the same type.[2]

Programming

Flowchart and program statements (Fig. 2) illustrate the ease of generating programs to control instruments. This program scans selected channels, programs the digital voltmeter to range and function, measures thermocouple voltage on each channel, converts this voltage to degrees Celsius, and prints results on the calculator's printer.

In the first step, six thermocouple coefficients are loaded into storage locations R_0 to R_5, for use in calculations which compensate for the thermocouples' nonlinearity. (These coefficients as listed are for an iron-constantan thermocouple.) The second step (statement 6) places the digital voltmeter in remote control, so that it can be programmed externally through the interface bus. Next, the voltmeter is programmed to the proper range and function. In the listing, for an HP 3490A digital voltmeter, the 2 sets the range to 100 mV and the 3 specifies direct voltage.

Up to this point, the system has been set up for making measurements and calculations, but has not actually made any. Before it can do so, the test operator must use interactive instructions to specify which channels are to be measured. An "Enter" statement causes the program to display the characters in quotes immediately following the statement, and to wait for the operator to enter information. In this case, the display is "Start Chan"; the operator enters the number of the channel at which measurements are to begin, and presses the Run key. Stop channel data are entered in the same manner.

The next statement measures the voltage on channel A and stores the measurement in memory location X. With the aid of a subprogram, this simple statement performs four functions: (1) sets scanner to specified channel; (2) takes a reading with the voltmeter; (3) transfers the reading into the calculator, storing it in memory location X; and (4) changes the data to fixed-point decimal form and rounds it to six places to the right of the decimal point.

Temperature is calculated using the nested polynomial to approximate the voltage-temperature coefficient of the thermocouple. Channel number and temperature are then printed and the program branches to measure the next channel. The channel number is automatically incremented as part of the "If" statement.

Rating Tradeoffs Between Programmable Calculator and Minicomputer

	Minicomputer					Programmable Calculator	
Parameter	Rank	Characteristic	Score*	Weight		Score*	Characteristic
Speed	2	Microsecond cycle time	2	1	0	0	Millisecond cycle time
Memory	4	Greater upward expandability Usually nonvolatile BASIC compiler takes 6K of memory	4	1	0	0	Usually volatile memory All memory available for program and data. Auxiliary memory available via disc and cassette
Cost	8	Requires peripherals to gain access	0	0	1	8	Built-in peripherals, diagnostics, editing. Can cost as much as 30% less
Ease of use	7	Requires compiler for software Additional hardware necessary to gain access	0	0	1	7	Resident compiler—requires no memory. Fixed algebraic or basic language. Convenient program generation and editing
Flexibility	5	Language flexibility— BASIC, FORTRAN, assembly	5	1	0	0	Limited, fixed-language, some ROM capability
Total	26		11			15	

*Score = Rank x Weight

Manual Data Acquisition

Former methods used to gather test data manually required a test engineer and two technicians—one to adjust and monitor the test-run parameters, the other to transfer temperature and pressure measurements onto forms, called "run sheets." A complete series of tests took a week or more. After correction and approval, run sheets were sent to the computer center for keypunching and processing through the data-reduction program. This data processing turnaround averaged another week following the tests.

Engineers cited several problems with the procedure, including (1) the sheer volume of numbers, and the limited amount of time and personnel available just to write them down; (2) the delay of up to two weeks in detecting measurement errors, which might become evident only after keypunching and processing, resulting in the loss of two weeks of testing and processing time; (3) the time and money spent on keypunching; and (4) the engineers' time, most of which was spent conducting test runs instead of planning new tests.

These difficulties called for a new testing approach, under some kind of automatic control. The problem imposed several requirements on the controller, including:

(1) Performing online data reduction

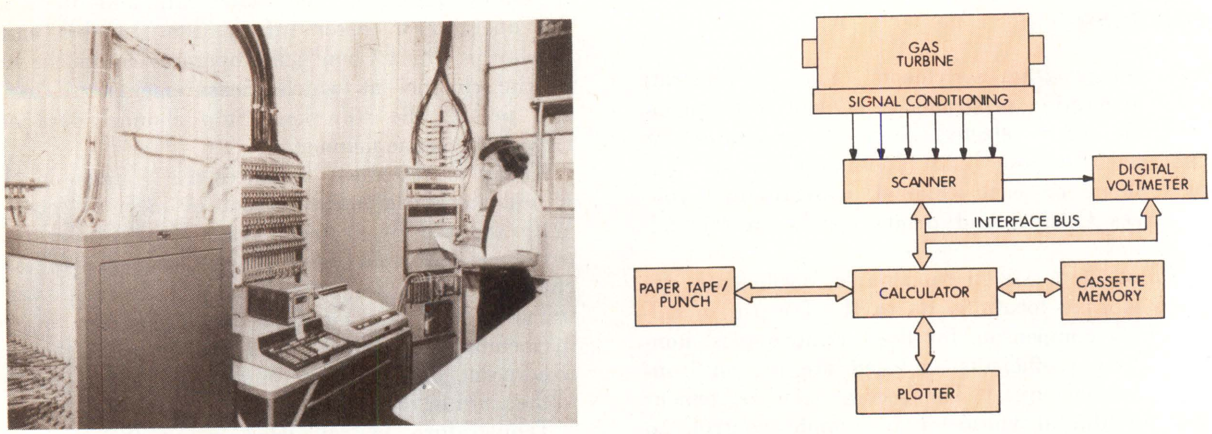

Fig. 3 System configuration. Calculator (center of photo) is brains of system monitoring transducers. Gray box at left is pressure multiplexer, fed from pressure junction box behind calculator; thermocouple leads are on rear wall. Cassette drive is on top of the calculator and plotter is beside it; other units (in block diagram) are located in the rack next to the technician.

(2) Linearizing transducer data

(3) Controlling all instruments

(4) Storing up to 18,000 individual data points

(5) Producing output on an X-Y plotter and on punched-paper tape

(6) Permitting easy program writing and modification

(7) Flexibility and expandability

The last requirement is satisfied by using instruments and a controller interconnected by a common interface[3,4] bus. In turn, this makes controller selection independent of the particular instrumentation, as long as it remains bus-compatible.

Several tradeoffs are illustrated in the accompanying Table. Parameters in the leftmost column are ranked more or less arbitrarily on a scale of 1 (least important) to 10 (most important) in this application. The two center columns give each of these a binary weight of 0 or 1 for each of the two alternatives, calculator or minicomputer, depending on which it favors. That weight is multiplied by the numerical ranking to give a score for that particular parameter; the sum of the scores provides a rough indication of which alternative is preferable. In this case, the calculator scores somewhat higher, although the margin is not large—36% higher than the minicomputer total and only 58% of the maximum possible score, given the arbitrary rankings.

Because the rankings are arbitrary, they apply only to this application at this time; clearly, the choice is largely subjective. Slightly different ranks and weights would shift the choice to a minicomputer.

System Configuration

The system configuration for the gas turbine project (Fig. 3) includes an HP 9820A calculator, with 5800 words of memory, cassette memory unit, digital plotter, digital voltmeter, paper-tape punch, and the previously mentioned scanner or multiplexer.

Program writing for the calculator is straightforward; with editing keys, program lines can be changed, added, or deleted. Cassettes hold previously written programs and data, storing up to 32,000 16-bit words per cassette—more than enough for the data storage requirement of 18,000 data points.

Preliminary plots such as the one shown (Fig. 4) insure that test data are valid during a test, and indicate necessary adjustments of test procedures. At the end of a successful run, a paper tape is punched with the results, for further processing at the company's computer center.

Although the calculator does not do all data reduction online, it does convert transducer input to engineering units, recalibrate all pressure channels, and warn of leaky channels in the pressure transducer, in addition to those functions mentioned previously.

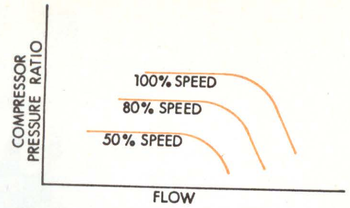

Fig. 4 Preliminary plots. Graphic output on calculator gives online indication that test is going well, before offline computer analysis is attempted

Conclusion

Introduction of a calculator-based data acquisition system has resulted in several major changes in the compressor test lab. Test time has been reduced from 2½ weeks to three days, while the amount of data gathered has increased by 40%. Turnaround has been reduced to less than one day, since the system, at the end of a successful run, punches a paper tape in standard format that is compatible with readers in the computer center.

Cost-justification was based on savings in keypunch time and operator time as well as on increased data output. Total system implementation and programming took less than six weeks.

Although Chrysler engineers chose to use the 9820A calculator, programmed in algebraic language through a numeric and function keyboard, the 9830A, which is programmed in BASIC, could have been used to permit operator interaction through a typewriter-like keyboard and alphanumeric display.

In instrument systems, the programmable calculator is attractive as a system controller. It can now do many jobs formerly reserved for minicomputers, including process monitoring and control, R & D lab design-verification and prototype testing, and multiparameter production testing. Its user-orientation and built-in high-level language have served to open the number-handling and computational power of the minicomputer to a much broader spectrum of users.

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2. "Thermocouple Measurements with the HP 3050B," Application Note #188, Hewlett-Packard Co, 1501 Page Mill Rd, Palo Alto, CA 94304
3. IEEE Standard 488, IEEE Standards Office, 345 E 47th St, New York, NY 10017
4. *Hewlett-Packard Journal*, Jan 1975

Jerry Estes holds a BSEE degree from the University of Colorado. Currently a product manager in the systems group of Hewlett-Packard's Instrument Div, his background includes experience in designing medical instrumentation and microwave communications equipment.

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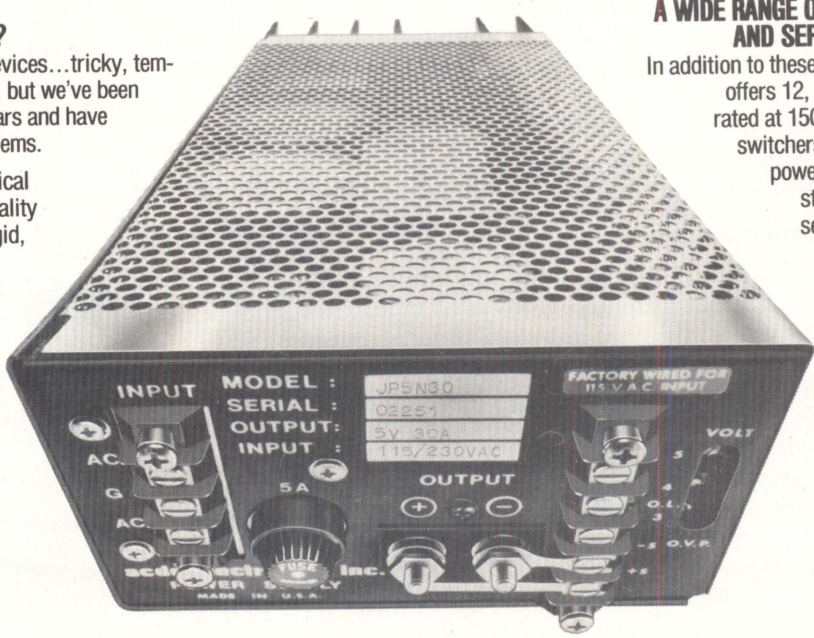

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Microprocessor users accustomed to hardware and puzzled by the art of executing a function with a program will benefit from generalizations based on software prepared for a lumber testing machine

Using a Microprocessor: A Real-Life Application

Part 2—Software

Lynn E. Cannon and Paul S. Kreager

Washington State University
Pullman, Washington

Software necessary to make a microprocessor-based system perform its intended function is frequently difficult for even skilled engineers to understand and to write, despite their experience in hardware design. To illustrate how such software is put together to execute a well-defined task, this article, the second in a 2-part series, describes the software in a lumber-grading machine built at Washington State University.

In Part 1 (*Computer Design,* Sept 1975, pp 69-77), the hardware implementation of the microprocessor-based system was described, including details on the microprocessor, interconnections, and operation of various components. Briefly, the tester (Fig. 1) induces a longitudinal stress wave and measures the time required to propagate the wave through successive 2-ft long segments of the specimen, computing the modulus from this elapsed time and the specimen's density. Thumbwheel switches specify the specimen's dimensions, and a load cell measures its weight. As the stress wave passes a sensor, a 1-MHz clock begins counting the time; at the next sensor, this counter turns off and the next counter turns on. Displays show the specimen's density, average modulus, and the lowest measured modulus, along with the location of the weakest segment as indicated by the low modulus.

Part 2 discusses the software, emphasizing concerns common to most users of microprocessors in general, but dealing with the Motorola MC6800 in particular, since the Washington State University project is based on this device. Little weight is placed on fine details of the particular software for the system.

Software requirements for the tester depend heavily on the system's input/output (I/O); in this case, all I/O is in binary-coded decimal (BCD) representation (see Table). After specifying the length, width, and thickness of the lumber to be tested, the system operator selects one of several different modes in which the system can operate, and depresses a start button. In normal mode, software collects dimension and weight information and issues a command to release the hammer and strike the lumber. After giving the hammer command, the software waits for an interrupt, signifying that the stress wave has passed all of the accelerometers; it then calls in the data from the counters, placing them in the read/write memory for processing.

After all input information has been stored, the microprocessor must evaluate several equations and display the results to the operator:

Software Input/Output

Software Inputs	Digital Format	Units
Function switch	FFFF	—
Length switch	LLL.L	in.
Thickness switch	T.TTT	in.
T-counters	TTT.	μs/2 ft
Weight	WW.WW	lb
Width	WW.WW	in.
Software Outputs		
Density	DD.DD	lb/ft^3
Modulus of elasticity	E.EE	lb x 10^6/in.^{2}
MOE low point	E.EE	lb x 10^6/in.^{2}
Location of low MOE	L	—
T-counter at low point	TTT.	μs/2 ft

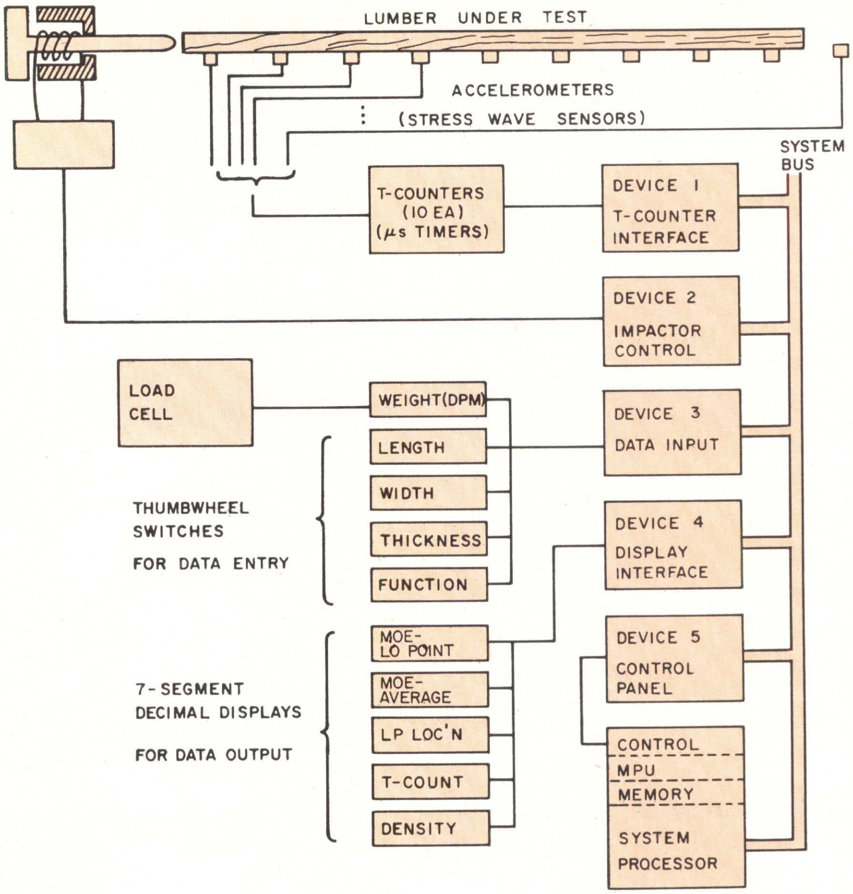


Fig. 1 Lumber grading machine. Software techniques for microprocessors are illustrated by this system, which computes the modulus of elasticity (stiffness) of a specimen of lumber from the velocity of a longitudinal compressive stress wave induced by a solenoid-operated hammer. Program releases the hammer, reads elapsed-time intervals from counters, and computes modulus of elasticity from these and from manually entered data

$D_1 = \frac{w}{LWT}$	Density in pounds per cubic inch, from the specified dimensions (L, W, T) and weight (w), for further computation
$D_2 = 1728\ D_1$	Density in pounds per cubic foot, the standard unit, for display
$MOE_n = \frac{kD_1}{T_n^2}$	Modulus of elasticity (MOE) for each segment of the specimen (up to 10) in millions of pounds per square inch; computed from the density and the inverse velocity (microseconds per foot) of the stress wave
$MOE_{LP} = \min\ (MOE_n)$	Lowest MOE in any segment (weakest part of the board)
$MOE_{avg} = \frac{1}{n} \sum_{1}^{n} (MOE_n)$	Average MOE for all segments of a single specimen

For display, all outputs, except location, consist of three or four digits with decimal point; the location output is a single digit indicating the section of lumber that has the lowest MOE value. Additional outputs provide abnormal result indications, including, for example, errors detected by the firmware, interrupt response failures, operator errors, divergent counter values, and power problems. If any of these are unrecoverable, yet another output tells the operator to reset the system and start again.

Since the system was composed of untested hardware and software, software design goals were formulated to minimize potential problems:

- Many tasks were written in modular form with arguments (data variables) passed through reserved areas in the read/write memory. While inline code is less difficult to write, isolating programming errors in it is more difficult. Modularity would have been less important in a smaller program [ours occupies 2048 bytes of read-only memory (ROM)].

- Programming shortcuts were avoided, even at the cost of additional space in ROM, so that those not intimately familiar with the software can follow its logic more easily. For the same reason, the symbolic-language listings contain many comments.

- A test program, written as an integral part of the software, serves three purposes: it aids initial hardware debugging of the system, assists operators check

```
        NAM   EXAMPL
        OPT   M
*
*   ADDRESS DEFINITION AREA
*
CNTRBD  EQU   $07FE          CONTROL BOARD ADDRESS = 07FE
   .
   .
*  .
        ORG   0              START OF RAM
*
*   FIRST 256 BYTES = DIRECT ADDRESSING AREA
   .
   .
*  .
        ORG   $00F9          STACK SAVE AREA
*
        RMB   1              MPU CONDITION AREA
        RMB   1              ACCUMULATOR B
        RMB   1              ACCUMULATOR A
        RMB   2              INDEX REGISTER
        RMB   1              PROGRAM COUNTER HIGH
STACK   RMB   1              PROGRAM COUNTER LOW
*
        ORG   $0800          START OF ROM
*
*   PROGRAM AREA
*
RESTRT
   .
   .
   .
IRQ
   .
NMI
   .
SWINT
   .
*
        ORG   $0FF8          MPU POINTER AREA
*
        FDB   IRQ            DEVICE INTERRUPT
        FDB   SWINT          SOFTWARE INTERRUPT
        FDB   NMI            NON-MASKABLE INTERRUPT
        FDB   RESTRT         RESTART ADDRESS
*
        END
```

Fig. 2 Software structure. Program begins with definition of I/O equipment and addresses, and specifies that storage begin at address 0. Pushdown stack is defined at end of 256-byte directly addressable portion of memory, followed by program. Fixed pointers for responding to interrupts are at end of program

for proper system operation, and when problems occur, helps maintenance personnel troubleshoot the system.

• To permit sections of code found to be in error to be patched without recompiling the entire program, blocks of no-operation (NOP) instructions were scattered throughout the program. Since this is not as easy as it sounds, the process will be described later.

Program Structure

While a program's structure depends heavily on the application, the basic structure of the program which was written for the lumber-grading machine (Fig. 2) demonstrates concepts that are applicable to many programs in general. For example, 256 bytes of read/write memory, with the address range from '0000' through '00FF' are directly addressed. (Addresses in hexadecimal notation appear in single quotes (') in the text, and are preceded by a dollar sign ($) in the listings. When neither mark is used, the notation is decimal.) In our preferred address structure, described in Part 1 of this article (*Computer Design*, Sept 1975, p 74), this directly addressed area of memory was followed by another, accessible with the extended address mode, up to '077F'; this upper area is not needed in the lumber tester, but remains clear. The next address is '0780', the first of up to 127 I/O devices; the 128th address, '07FF', is reserved for a dummy device that is "read" in response to an interrupt. All I/O devices, therefore, have addresses of the form '07mn', where m ranges from '8' to 'F' and n from '0' to 'F'. Finally, the program itself begins at '0800' and ends at '0FFF', a 2048-byte area usually implemented in ROM.

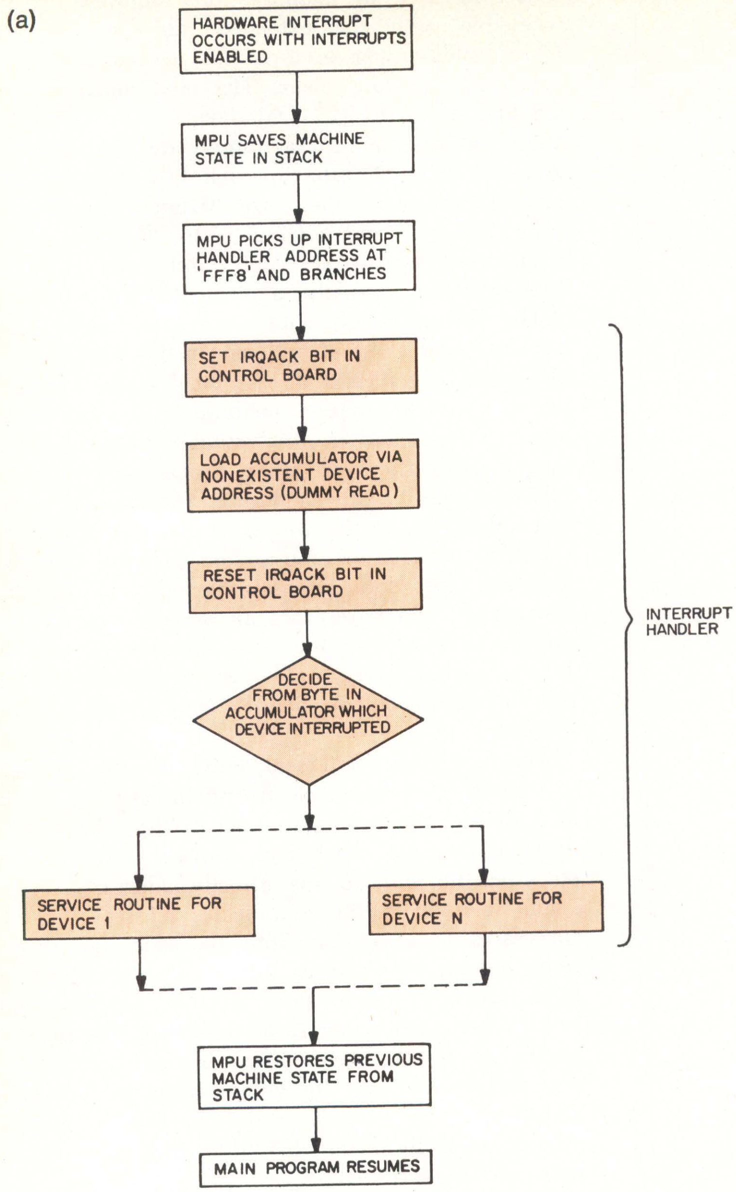
The listing begins with a program name (such as EXAMPL) and a list of options (in this case, only option M—which specifies that assembled code is reproduced on a specified output medium such as printer or punched tape, and is also retained in the memory, so that a simulation or other process can immediately follow assembly. Other options are available with most assemblers, specifying the exact machine configuration, available peripherals, and so on.) Device addresses are assigned with EQU, an assembler directive or pseudo-instruction, which replaces all occurrences of the symbolic addresses with the assigned numerical addresses. In the partial listing only one such address is shown, that of the control board, symbolically designated CNTRBD.

The first origin statement, ORG, directs the assembler to store the machine-code listing in memory, beginning at address 0, to take advantage of the microprocessor's direct-addressing capability. Another ORG places the stack at the end of this directly addressed area; the symbolic address STACK indicates address '00FF', and successive bytes pushed into the stack go into locations having successively lower addresses. Since seven bytes are required to store all the data that must be saved when responding to an interrupt, the second ORG begins at '00F9' (seven bytes beginning at this location end at '00FF'). Individual items in the stack are identified by the directive RMB (Reserve Memory Byte) accompanied by a number that indicates how many bytes should be reserved.

While only the stack shown was implemented in the lumber tester, a small buffer area was left in the memory immediately preceding the stack as a precaution against possible software or hardware errors that might prevent the stack pointer from being reset, thus destroying data in the memory. This precaution would fail in microprocessors where the stack pointer normally loops from the end of the stack area to the beginning, if the pointer were to keep on decrementing; but it can prevent destruction of data by any occasional mishandling of the stack pointer.

ROM program area is next; it begins with a third ORG, to '0800'. The program itself is not shown here; however, the four symbolic addresses are entry points to user's routines that begin at the hardware-defined interrupt and restarting addresses. The microprocessor unit (MPU) is internally designed to address four predefined areas among the highest addresses in the range when these events occur; the ORG to '0FF8' defines the last eight bytes to be used for this purpose. FDB is another assembly directive which "Forms a Double Byte."

For example, a device interrupt causes the MPU to branch to location 'FFF8', which turns out to be



(b)

```
*       DEVICE  1  RETURN BYTE = 01
*       DEVICE  2  RETURN BYTE = 02
CNTRBD   EQU       $07FE          CONTROL BOARD ADDRESS
DUMMY    EQU       $07FF          DUMMY ADDRESS
   .
   .
   .
*       INTERRUPT HANDLER
*
IRQ      LDA   A   #$04           IRQACK BIT ON
         STA   A   CNTRBD         SET IRQACK LATCH
         LDA   A   DUMMY          GET INTERRUPTING ADDRESS
         CLR       CNTRBD         RESET IRQACK LINE
         CMP   A   #01            DEVICE 1 INTERRUPT ?
         BNE       SKIP           NO, GO SEE IF DEVICE 2
         JMP       SERVD1         YES, GO SERVICE
SKIP     CMP   A   #02            DEVICE 2 INTERRUPT ?
         BEQ       SERVD2         YES, GO SERVICE
         JMP       ERROR          NO, ERROR CONDITION
   .
   .
   .
SERVD1                            SERVICE DEVICE 1
   .
SERVD2                            SERVICE DEVICE 2
   .
ERROR                             SERVICE ERROR CONDITION
```

Fig. 3 Interrupt handler. Flowchart (a) shows general form of MPU's response to interrupt from one of several devices. Blocks in color correspond to detailed listing (b), which shows how MPU determines which of two devices caused interrupt

a pointer to IRQ, the address of the beginning of the routine that services the device interrupt. Although the MPU executes a branch to an address with the most significant four bits true, shown by the first of the three F's in the hexadecimal address, the ROM is wired to ignore those bits and to use the address '0FF8' instead.

A similar response follows the Software and Non-Maskable Interrupts (SWI and NMI). The fourth predefined area, RESTRT, is entered whenever the power passes from a low to a high state. In general, this address is set at the start of the program where the software initialization takes place.

As mentioned earlier, blocks of NOPs were inserted at intervals throughout the program. Care is required in choosing where to insert them, to avoid difficulty with relative branches, for example. We used blocks containing from two to eight NOPs—the larger blocks in areas that were judged to have a higher probability of errors. These blocks provide space for insertion of instructions to correct erroneous sequences without having to change addresses throughout the program. If ROM consists of several integrated circuit (IC) packages, this scheme also allows errors to be corrected in only those chips that contain the error, without recoding the entire ROM.

Special-Purpose Routines

In the lumber tester, interrupts are handled using an interrupt acknowledge, rather than with the software polling scheme, as suggested in MC6800 literature. Details of the interrupt response are described in Part 1 (p 72). Essential steps in the associated software (Fig. 3) check for one of two possible interrupts. If neither is valid, the program transfers to an error routine.

Upon recognizing an interrupt condition, the MPU disables further interrupts and branches to the interrupt handler routine. Accumulator A is loaded with '04', which is all 0's except the third bit from the right end. This byte is then sent to the control board—that is, it is "stored" in the location occupied by the control board. The solitary 1 in this byte sets the interrupt acknowledge (IRQACK) latch. Accumulator A is then loaded with the interrupting device address via the dummy read. As described in Part 1 and previously in this part, no device responds to the symbolic address DUMMY except when it has highest priority among those devices that caused an interrupt. After acquiring the interrupting address, the control board is cleared, turning off the IRQACK line. The remaining compare, branch, and jump instructions in the routine determine which device caused the interrupt. A number sign (#) specifies an immediate address.

Generally, after this routine has been executed, interrupts are re-enabled. Again, it is important to recognize that the return byte for the dummy read can be set up to represent an address, number, index, or anything with a specific meaning relative to a particular interface.

Likewise, BCD algorithms using the Decimal Adjust Accumulator (DAA) instruction can be confusing. An example of such an algorithm implements BCD division with repeated Subtract (SUB) and DAA instructions. It is based on a prenormalized restoring algorithm, in which each digit of the quotient is generated by counting the number of times the divisor must be subtracted from the dividend to obtain a negative result. When the negative result appears, the quotient count is complete, so the divisor is added (restored) once. The sum is the remainder, if the quotient's last digit has been counted up; otherwise, it is shifted left and the process is repeated.

As implemented in the lumber tester, the quotient is a fixed-point BCD number with an extra binary byte containing the decimal point displacement. If necessary, divisor and dividend are normalized by shifting left one digit at a time until the most significant digits of both numbers are nonzero. (If the divisor is small, normalization gives it a string of trailing 0's.)

In the process of successive subtractions, beginning after normalization, SUB will not work with the DAA instruction, as pointed out in the description of the instruction set (see "MC6800 Instruction Set," p 87). Therefore, instead of subtracting the divisor, the 10's complement of the divisor is added; the 10's complement is obtained by replacing each digit of the divisor with the difference between it and 9, and adding 1 to the resulting number. Equivalently, the extra 1 is added first, simplifying the instruction sequence. (Again, the complement of a small normalized divisor has a string of trailing 0's).

In each subtraction, the whole 8-digit divisor is subtracted from the whole dividend. However, since the 8-bit microprocessor can accommodate only two digits at a time, several passes through an inner loop are required for each individual subtraction. One such subtraction increments one digit of the quotient; if the difference is still positive, there is an iteration through an outer loop that repeats the several inner loops. After one digit of the quotient has been counted up to the proper value, the dividend is shifted one place to the left and the whole process of inner and outer loops is repeated for the next digit of the quotient. A separate index register keeps track of which quotient digit is accumulating.

The key idea in the algorithm, the central part of which is detailed in Fig. 4, is use of the DAA instruction to convert the results of adding decimal numbers, which the hardware interprets as binary, and use of a complemented-add instead of subtraction, since the DAA will not work following the latter. The program first clears the memory location in which the digits of the quotient will be collected. Then the carry-bit, part of the condition-code register, is set to 1, starting the routine's outer loop, in preparation for forming the 10's complement of the divisor. As are other quantities in the system, the divisor and dividend are basically 8-digit numbers before normalization, after normalization, two digits are added at the high-order end of the dividend, making it a 10-digit number, to insure that the negative result is detected at some point following repeated subtraction of the divisor. Both extra digits are 0. The process subtracts two digits (one byte) at a time, so that the whole length of the 10-digit dividend is serviced by five subtractions in an inner loop, generating one count of the quotient; thus the number 5 is placed in the index register.

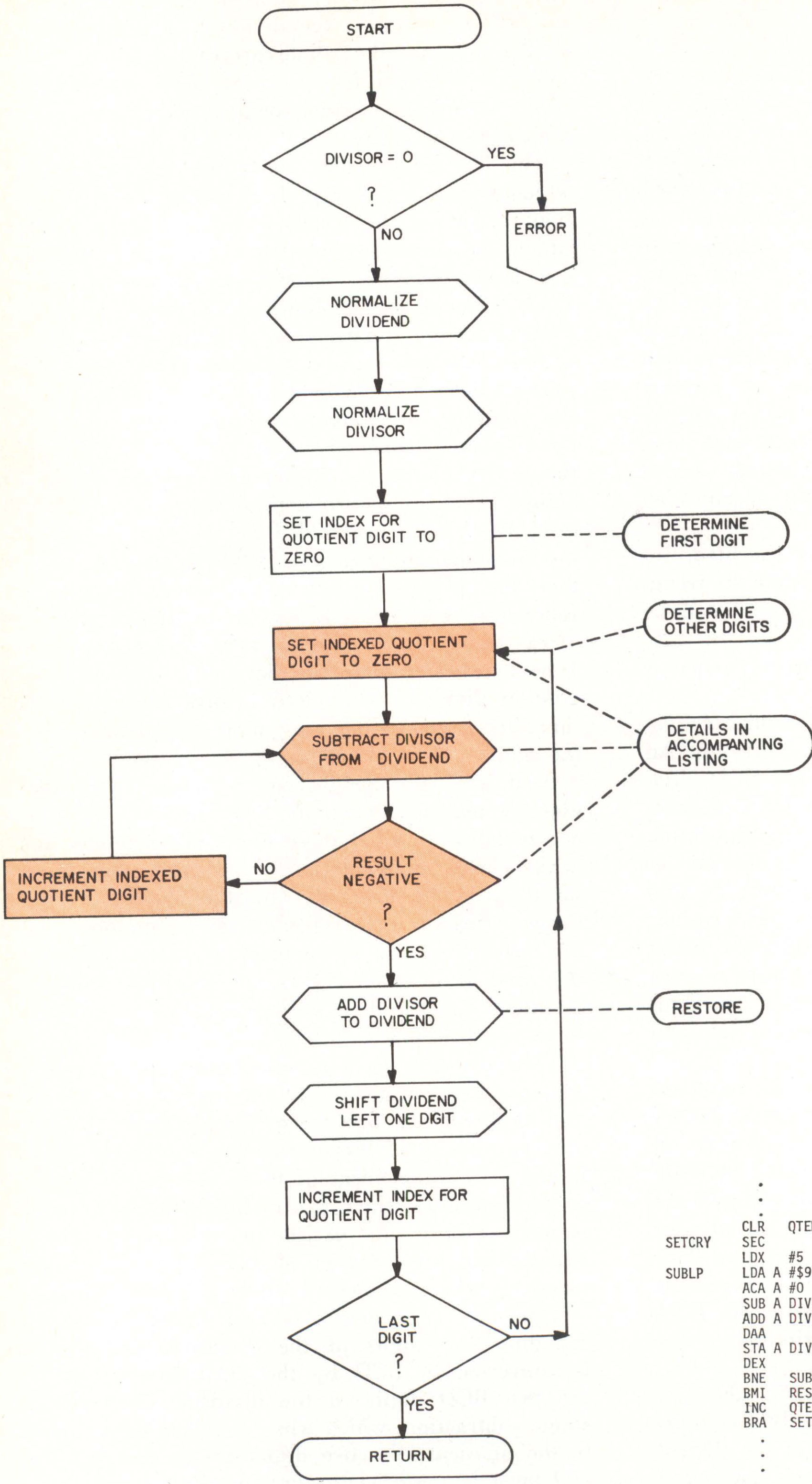
Next, the 10's complement is formed. This step begins by placing the number '99' in BCD form in the accumulator. In BCD these digits are identical to their hexadecimal representations; therefore, they must be specified in hexadecimal (by the symbol $) in the listing. Hexadecimal specification is important, since the instruction uses the immediate address (the symbol #), and if hexadecimal is not specified, the number 99 would be placed in the accumulator in pure binary form, which would be incorrect.

Then the number 0 is added with the carry—which simply adds the previously set carry-bit to the 99 in the accumulator, producing hexadecimal '9A'. From this, two digits of the divisor are subtracted, resulting in the 10's complement of those two digits. The index register specifies which two of the 10 digits are complemented. (When the divisor is small and the index register has been decremented no more than once or twice, these complemented digits are likely to be 00.)

This 10's complement is now added to the corresponding two digits of the dividend, and the result is converted to BCD by the DAA instruction. These are two BCD digits of the dividend after part of a single subtraction, which when complete adds one count to the quotient; the two digits are in the accumulator and must be restored to corresponding positions in the dividend—achieved with the Store Accumulator (STA) instruction, indexed as before.

SUB, ADD, and STA instructions in the listing do not address the divisor and dividend as such, but instead point to locations immediately to their left, as modified by the index. Since the symbolic address DIVISR points to the most-significant byte (two most-significant digits) of the divisor, and since the con-

(a)



(b)

```
                .
                .
                .
         CLR    QTEMP          CLEAR THE QUOTIENT DIGIT
SETCRY   SEC                   SET THE CARRY BIT
         LDX    #5             INDEX POINTS TO BYTES IN DIVISOR AND DIVIDEND
SUBLP    LDA A #$99            LOAD ACCUM. WITH 2 BCD 9'S
         ACA A #0              ADD THE CARRY BIT
         SUB A DIVISR-1,X      SUBTRACT TO GET TEN'S COMP. OF DIVISOR
         ADD A DIVIDN-1,X      ADD DIVIDEND TO GET THE DIFFERENCE
         DAA                   DECIMAL ADJUST TO GET GOOD BCD
         STA A DIVIDN-1,X      PUT THE DIVIDEND BYTE BACK
         DEX                   DECREMENT THE INDEX
         BNE    SUBLP          LOOP UNTIL DONE
         BMI    RESTOR         IF RESULT NEG. GO RESTORE
         INC    QTEMP          IF NOT COUNT THE SUBTRACT
         BRA    SETCRY         AND GO SUBTRACT AGAIN
                .
                .
                .
```

Fig. 4 BCD division. Outline of entire algorithm is in flowchart (a), beginning with elimination of leading 0's in dividend and divisor, and showing how quotient is determined one digit at a time by successively shifting the dividend to the left. Each quotient digit is determined by counting number of subtractions of divisor from dividend necessary to obtain negative result (colored blocks). Because microprocessor works in binary, this requires use of DAA instruction to restore result to BCD; because DAA will not work with subtraction, process requires that the divisor be complemented and added, as shown in detailed listing (b)

MC6800 Instruction Set

The MC6800 offers the programmer an extensive set of instructions (see Table), which range in length from one to three bytes, as well as hardware features that include two 8-bit accumulators, a 16-bit index register, a 16-bit stack pointer, and a 6-bit condition-code register.

Six different addressing modes enhance programming flexibility:

Immediate—Operand (data processed by the instruction) forms part of the instruction, appearing in the second or second and third bytes of the instruction.

Direct—Second byte of the instruction contains the operand's address. The operand must be stored somewhere within the first 256 bytes of read/write memory, since that is the maximum space addressable by a 1-byte address.

Indexed—Contents of the index register are added to contents of the second byte of the instruction; the sum is a 16-bit operand address. The 16-bit address allows the operand to be stored anywhere in memory, which can have a capacity of $2^{16} = 65{,}536$ bytes.

Extended—Second and third bytes of the instruction form a 16-bit address of the operand in memory. The extended address is like the direct address except that its length removes the location restriction on the latter.

Implied—Instruction implies the location of the operand; for example, DECA decrements accumulator A.

Relative—(Used only for branch instructions.) Contents of the second byte of the instruction constitute a displacement that is added to or subtracted from the program counter.

Direct mode allows the first 256 bytes of memory to be accessed more rapidly than the rest, because the second byte of the address need not be fetched. However, not all instructions can use this mode; those that cannot include clear, increment, decrement, test, complement, negate, and all shift and rotate instructions.

Indexing can trip up the unwary programmer because only one byte is added to the 2-byte index register. In many computers, the address part of an instruction indicates one end of an array of data somewhere in memory, while the index register contains a small number that defines the exact point in the array where processing is currently taking place. As the computer reiterates a loop of instructions, the index register decrements; when it reaches 0, control passes out of the loop to another program subroutine. In the MC6800, however, the index register holds such a large number that the programmer must take care that its contents, when added to the address in an indexed instruction, do not take the program out of the first 256 bytes of memory. While an indexed array could be elsewhere, if necessary, the index register would then have to carry a constant displacement—that is, the loop would end when the register decremented to a prescribed number, possibly large and certainly not 0.

Condition-code register bits indicate interrupt mask, negative, zero, overflow, carry, and half-carry—a carry from the low-order to the high-order digit in BCD mode. They are set or cleared according to the result of instruction execution. Since not every condition code is changed by every instruction (details are given in MC6800 documentation), problems may arise if the programmer is not aware that, for example, the test instruction clears the carry and overflow bits, that decrement index does not affect the negative bit, or that compare index does not work with some conditional branches.

The MC6800 has no input/output (I/O) instructions; instead it treats device registers as if they were memory locations, somewhat in the manner of the Digital Equipment Corp PDP-11 minicomputer. Since most instructions can act on operands in memory without first moving them to an accumulator, I/O is straightforward.

Binary-coded decimal (BCD) arithmetic is simplified by the Decimal Adjust (DAA) instruction, which follows a binary addition of two bytes (each consisting of two BCD digits) and adjusts the result to form the correct BCD sum and carry. Since DAA does not work following a subtract, however, BCD subtraction requires a 10's complement and an add and DAA.

Subroutine calls are simplified by the Branch to Subroutine (BSR) and Jump to Subroutine (JSR) instructions, which store the contents of the program counter in the pushdown stack—a reserved section of memory. Return from Subroutine (RTS) restores the most recently stored program address to the program counter. Similarly, interrupts automatically save the six condition codes and contents of accumulators, index register, and program counter in the stack, and transfer control to an interrupt address. Only one external interrupt address is available in the MC6800, which can not distinguish between different kinds of interrupts and branch to different addresses. Return from Interrupt (RTI) restores all this information.

The Software Interrupt (SWI) instruction stores the same information in advance of an external interrupt, but branches to its own interrupt address. Wait for Interrupt (WAI) saves the information in the stack and suspends execution until an external interrupt occurs. This instruction speeds response to an expected interrupt by skipping the stacking cycles.

Three MC6800 instructions were known to cause problems (at the time this article was written). Clear Interrupt Mask and Set Interrupt Mask create a problem if they are preceded by certain byte values fetched from ROM; Software Interrupt also causes a problem under certain specific conditions. Users should contact Motorola to obtain the latest information on these problems.

tents of the index register are added to the numerical equivalent of this address, the −1 is required to insure that the correct digits are involved in each iteration. For example, on the first iteration through this loop, if DIVISR were specified and indexed, subtraction would take place on the byte with the address DIVISR + 5, whereas the least-significant digits of the divisor are in DIVISR + 4.

Since two digits of the original dividend have been replaced with two others following a partial subtraction, the index register is decremented. If this decrement leaves a nonzero number in the register, subtraction is not yet complete; the routine returns to the start of the inner loop, reloading 99 into the accumulator to obtain the 10's complement of the next two digits. On the other hand, if the index register now contains 0, subtraction is complete. If the most recent addition of the complemented divisor left a positive result, another subtraction is necessary; 1 is added to the quotient count and another outer loop is undertaken. However, if two 9's have appeared in the two extra digit positions at the high-order end of the dividend, the result is recognized as negative, the quotient count is omitted, and the program branches to a separate routine to restore the divisor. Two 9's in binary are 1001 1001; the leading 1-bit is the negative

Instruction Set

Mnemonic	Instruction Description
ABA	Add Accumulators (not with carry)
ADC	Add with Carry
ADD	Add
AND	Logical AND
ASL	Arithmetic Shift Left
ASR	Arithmetic Shift Right
BCC	Branch if Carry Clear
BCS	Branch if Carry Set
BEQ	Branch if Equal to Zero
BGE	Branch if Greater or Equal Zero
BGT	Branch if Greater than Zero
BHI	Branch if Higher
BIT	Bit Test
BLE	Branch if Less or Equal Zero
BLS	Branch if Lower or Same
BLT	Branch if Less than Zero
BMI	Branch if Minus
BNE	Branch if Not Equal to Zero
BPL	Branch if Plus
BRA	Branch Always
BSR	Branch to Subroutine
BVC	Branch if Overflow Clear
BVS	Branch if Overflow Set
CBA	Compare Accumulators
CLC	Clear Carry
CLI	Clear Interrupt Mask
CLR	Clear
CLV	Clear Overflow
CMP	Compare
COM	Complement
CPX	Compare Index Register
DAA	Decimal Adjust (accumulator A only)
DEC	Decrement
DES	Decrement Stack Pointer
DEX	Decrement Index Register
EOR	Exclusive-OR
INC	Increment
INS	Increment Stack Pointer
INX	Increment Index Register
JMP	Jump
JSR	Jump to Subroutine
LDA	Load Accumulator
LDS	Load Stack Pointer
LDX	Load Index Register
LSR	Logical Shift Right
NEG	Negate
NOP	No Operation
ORA	Inclusive-OR Accumulator
PSH	Push Data
PUL	Pull Data
ROL	Rotate Left
ROR	Rotate Right
RTI	Return from Interrupt
RTS	Return from Subroutine
SBA	Subtract Accumulators (not with carry)
SBC	Subtract with Carry
SEC	Set Carry
SEI	Set Interrupt Mask
SEV	Set Overflow
STA	Store Accumulator
STS	Store Stack Pointer
STX	Store Index Register
SUB	Subtract
SWI	Software Interrupt
TAB	Transfer Accumulators
TPA	Transfer Condition Code Register
TST	Test
TSX	Transfer Stack Pointer to Index Register
TXS	Transfer Index Register to Stack Pointer
WAI	Wait for Interrupt

indication, which sets the sign bit in the condition code. These digits will always be 9 when the subtraction produces a negative result, so that the leading bit will always turn to 1 at this moment. If the two extra leading digit positions had not been added, the last subtraction might have produced a result having a first digit of less than 8 or 9; the microprocessor, basically a binary machine that can do BCD arithmetic with the aid of the DAA instruction, would not recognize such a result as being negative.

Restoration is shown in the flowchart but not in the listing. It adds the true divisor to what remains of the dividend.

Application Software

The program structure, interrupt routine, and BCD division routine described to this point are generally useful in many applications. Specific software for the lumber-grading machine includes, for example, a power-up restart vector, which transfers to a routine that clears the memory, initializes console lamps and displays, and generates a programmed reset through the control board. The machine is then ready, with interrupts enabled, but not processing until the operator generates a command from the console.

Similarly, the power-fail vector, a non-maskable interrupt (NMI), transfers to a routine that turns on two console lamps, indicating the error and telling the operator to reset the machine. These are important in short-duration power glitches, which might cause a problem since the operator would not otherwise be aware of them. An appropriate power-failure detector in hardware is necessary to utilize this routine.

Routines that test the displays require a time interval between changes so that the operator can visually check their operation. They use the software interrupt instruction (SWI) to transfer to a routine that generates a 1-s time delay. The same instruction can be used wherever else this delay is required—for example, to delay execution of the ROM testing routine until the operator has had time to remove his finger from the start button after initiating the test.

The prototype lumber-grading machine was designed as a research project involving many computational steps in the software. Future machines for commercial use based on this system could be restricted to lumber with standard dimensions. Such a restriction would eliminate the necessity for many calculations by performing them with tabular methods. For instance, dimensions and weight of standard lumber could serve as indexes to a table containing density values, eliminating two of the five equations previously listed.

Software Development

Development of software for a microprocessor generally involves the use of another computer. This may be a large batch or time-sharing system, a minicomputer, or a developmental system based on the microprocessor itself. MC6800 software support, including such items as a cross-assembler and a simulator, was available through the General Electric and United Computing Systems time-sharing services at the time this article was written. Batch versions were also available. All these systems cost money; for small programs, hand-compilation may be less time-consuming and cheaper in the long run.

With time-shared systems, assembly-language instructions are entered through a local terminal into a remote computer, and are edited as required. Then, using the same terminal, support packages resident on the computer are invoked to assemble and simulate the program. Other packages, available through the terminal, aid software development still further. These same software support packages may also be purchased to run in batch mode on the user's own computer facility; this may be less costly when users anticipate doing a substantial amount of software work with a particular microprocessor.

Charges for time-sharing service vary between vendors and depend on computer time used, file storage, terminal connection time, and amount of terminal I/O performed. There is generally an initial charge to the user for gaining access to the system; in some cases, there may be a minimum monthly charge for services. Some microprocessor chip manufacturers also put a royalty on computer time, which shows up in the billing to the user.

Accumulated software development costs can become quite significant with a sizable program. For example, even when using cost-cutting techniques, entry, assembly, and listing of a 2-kilobyte program for the lumber-grading project cost approximately $100 *per run*. Needless to say, some users cannot afford many program errors at those rates.

Benchmark comparison of two time-sharing services offers a better understanding of the potential costs. A 60-byte program containing no errors was entered, compiled, and listed by both previously named services under the same conditions. While I/O charges were 38% cheaper on one system, computer time charges were 36% cheaper on the other. However, since the generality of a benchmark is difficult to judge, potential users may profit by shopping around among various services, considering whether their needs are more I/O or computation bound.

Cost Cutting

To reduce costs, we developed our software on an in-house IBM 360/67 using a conversational text editor called WYLBUR. The program was entered, edited, and filed. Then, using editing capabilities, a shortened version of the program was placed in another file, with all comments and unnecessary blanks deleted. This version was copied onto a local cassette tape and then read into a remote time-sharing system, thereby minimizing both errors and the time required for entry. The remote computer assembled the program and sent the output back to the local cassette tape. Finally, this tape was read into a third file on the local 360/67 and merged with original source code to produce a listing complete with comments and object code.

To reduce software development costs even further, a simple simulator for the MC6800 checked out portions of the microprocessor software on the in-house computer. The simulator repeatedly dumps selected portions of the memory as execution progresses, giving a series of "snapshots" of the process. While not as convenient as an interactive simulator, this simulator could make many runs for the cost of one run on a time-sharing system.

Conclusions

With a few minor exceptions, the instruction set of the MC6800 is well laid out and easily learned. Persons having only limited experience in programming should not be dissuaded from using this chip, especially for projects having small to moderate coding requirements. However, care should be taken to choose an appropriate interrupt scheme, which will minimize problems in coding space and response time. Also, although the MC6800 has a DAA instruction, decimal arithmetic is sometimes troublesome, requiring a considerable amount of storage and posing problems in keeping track of the decimal point. For relatively large software requirements, as was the case in this project, developmental costs of software can equal or exceed the investment in hardware.

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Reference

"MC6800 Microcomputer Reference Manual," Motorola, Inc, Semiconductor Products Div, 5005 E McDowell Rd, Phoenix, AZ 85008

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Lower costs and higher reliability in optical character recognition bring data entry systems into a new developmental phase that utilizes marketing, mathematical, and engineering skills

OCR System Design Benefits from Technological Advances

Richard K. Dove

Ball Computer Products, Incorporated
Oakland, California

Technological advances have recently enabled optical character recognition to enter a new phase of development. These advances offer the system designer considerably lower costs and higher reliability and accuracy—a new cost-effective solution to old data entry problems.

Furthermore, as part of this phase, both systems and product designers have learned that they cannot assure success by simply applying the latest state-of-the-art components and techniques. They now realize that success is most likely to result from an integrated design team that combines the skills of engineers, mathematicians, and marketing people.

This phase-transition results from advances in paper transports, in scanners and digitizers, and in recognizers—as well as in system integration. Transports bring the document into position for data entry; scanners and digitizers transform data on the document into patterns of electrical pulses; and recognizers interpret those patterns and translate them into conventional standard codes for further processing.

Advances in Paper Transports

One of the problems that mechanical designers live with has been aptly expressed: "There is no such thing as mechanical hi-fi." These mechanical limitations must be tolerated in many electronic systems, including optical character recognition (OCR) devices, where serious difficulties arise from the mechanics of paper movement, the source of most machine failures. For example, a machine cannot scan documents any faster than it can unstack and restack them. Although it can work faster with heavy paper or card stock, it should be able to accommodate less expensive and lighter papers, including common bond, which have irksome aerodynamic qualities.

Vacuum and friction belts, previously not feasible in many designs, can now be useful if they are made from certain new materials that are based on synthetic fibers impregnated with natural or synthetic rubber. In particular, rubberized nylon is such a material; another is neoprene with dacron. Both of these are very strong, and have good friction characteristics and long wear.

For example, one simple paper-feeding mechanism uses four ½-in. wide belts, side by side, that extend into the top margin area of a stack of forms placed facedown directly on the scanner (Figs. 1 and 2). After the bottom sheet has been read, the friction belt pulls it out of the scanning area, through a gate adjusted to let a single sheet pass but not two. This belt mechanism functions as both picker and transporter; documents need not be moved before scanning. The weight of the stack itself, with perhaps a cap to hold down the last few sheets, is the force that creates the friction against the belt. If the transport mechanism fails, documents may be manually placed on the scanner; unfortunately, if the scanning mechanism fails, the transport is useless.

Other mechanisms feed the top sheet from the stack, which must rest on a pallet that rises as the stack diminishes in height (Fig. 3). In general, these mechanisms require that the sheet be moved into position for scanning, and then moved out to make room for the next sheet.

Nevertheless, moving paper, even at low speeds, makes the registration problem difficult. To maintain rigid and positive control over a moving piece of paper,

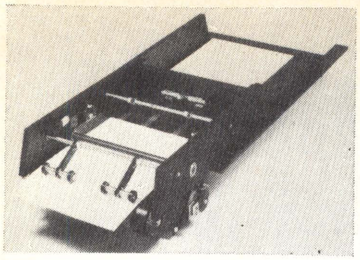

Fig. 1 Simple transport assembly. Success of this method of moving paper in an optical character reader is due in part to a new high-friction material used in the four belts that carry the paper

mechanisms must be designed with such close tolerances that the incidence of mutilated documents rises sharply.

Since any device that moves documents is subject to jamming, the product designer must not only make paper-jam clearing easy, but must also keep such jams and other single-point failures from seriously affecting the system's throughput. Most downtime of electronic systems is attributed to its mechanical portions—in an OCR system, the paper mover. As OCR equipment cost continues to decrease, instant service response by resident engineers grows less economical. Thus, to protect installations that cannot tolerate downtimes of more than 15 minutes or so, an OCR system's paper-transport mechanism should be designed so that, if it fails, documents can be manually placed for scanning.

One way to bypass some paper handling problems is to keep the paper stationary and move the scanner. Although scanners in the past have required solid mounting, the advent of plastic lenses, which make optical systems much lighter, as well as other weight savings that are possible with the newer solid-state electronic devices, have made the use of moving scanners feasible.

However, moving the scanner introduces a new problem: finding a way of getting electrical signals from the moving scanner to the rest of the system, which remains stationary. This can be done using flat cables, developed to withstand many million flexings before failure. These cables are used, for example, in IBM's 3886 and in the Ball Computer Products OCR 7600, both of which use mechanically moving scanners.

Advances in Scanners and Digitizers

In its simplest form, a scanner consists of a light source, a means of directing the light over the two dimensions of a document, an optical subsystem to form an image from the reflected light, and a light sensor to detect the resulting image. The scanner must also be capable of correlating each sample of reflected light with the coordinates of the position on the scanned document from which it was obtained. The source must provide enough light in the short time allowed, limited by the instantaneous character recognition rate, to insure a good signal-to-noise ratio in the sensor and to permit adequate resolution in the digitizer, while not exceeding the amount of heat that is allowable.

In recent years, beginning with the invention of the laser, many new components have been developed that improve scanner technology. The most interesting advances have come in solid-state technology, including silicon junction diodes, self-scanned linear arrays, light-emitting diode arrays, TTL-compatible phototubes, silicon photodiodes with modified spectral response curves, and hybrid packaging of photosensing devices. Others, however, are not to be discounted, such as fiber optics, high resolution vidicons, and optical shaft encoders. These developments increase scanning speed, improve

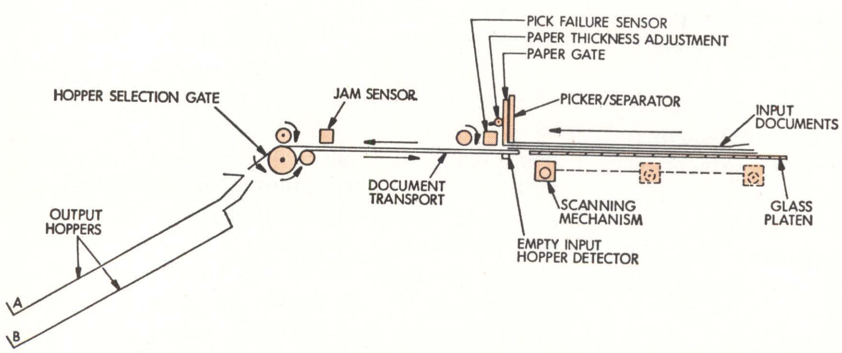

Fig. 2 Paper transport mechanism. Cross-section of assembly pictured in Fig. 1 shows how documents are scanned before being moved. Stack of documents is placed facedown on glass platen; scanner moves under glass to read data from bottom document. After scanning, picker pulls bottom document from stack; transport deposits it in one of two output hoppers, usually depending on whether it was read successfully

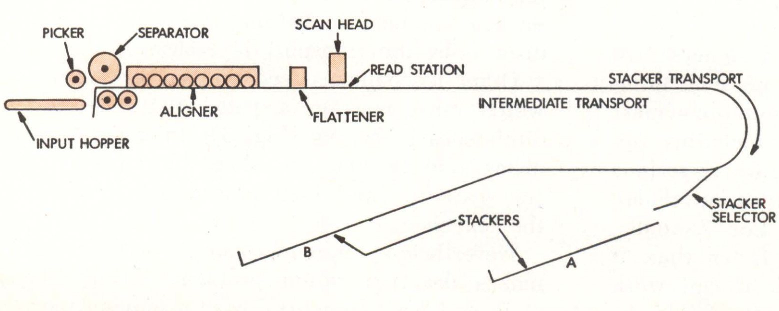

Fig. 3 Alternative transport method. Some OCR machines remove top document from stack, pull it under a scanner (read station), pause for reading, then drop it into one of two or more output hoppers

resolution, and reduce the size and weight of the scanner—the last opening up possibilities for moving subassemblies. Eventually, volume production of these components will considerably reduce associated manufacturing costs.

One of the primary problems in choosing a light source is obtaining enough illumination without generating too much heat. A significant advance in this respect, the laser, produces an extremely narrow beam of coherent light and does not waste power; it concentrates the full power of the light source on that portion of the document which is being illuminated, losing none to the surrounding area. Additional advantages of the laser are that the light beam itself can be directed to effect the actual scanning; the usual red light is well suited to silicon junction sensing, thus using energy efficiently.

Primary drawback of the laser is the danger that its beam will enter someone's eye, causing severe damage or blindness; consequently, it can generate an uncomfortable feeling in the minds of operators and other personnel near the machine, even when the beam is shielded. Lasers also tend to make production machines difficult to ship and install.

Flash tube technology has been refined to a state that may lead to a significant breakthrough. For instance, a flash tube could be used in conjunction with a high resolution vidicon in a high speed OCR system. As documents are moved continuously past a scan area, a high speed strobe unit would illuminate the entire document; the vidicon would capture all the data instantly, and scan it electronically while the next page is moved into position.

Tungsten filament bulbs have become brighter, smaller, and lighter, all concurrently; their output wavelength is suitable for sensing in a silicon junction. Their small size makes them suitable for use in mechanical scanners previously mentioned.

Light-emitting diodes produce wavelengths well matched to those sensed by silicon junctions and, like lasers, use energy efficiently. They are available in linear arrays, which can be coupled with a single sensor [as in the IBM 3886 (Fig. 4)] to achieve a scanning digitization that is the inverse of the digitization of an array of photodiodes coupled with a single light source (as in the Ball Computer Products OCR 7600).

Scanning the Document

Light can be sensed from various points on a 2-dimensional document in any of several ways. In some applications, the problem is considerably simplified if only one or two lines on each document must be read. If these documents contain many lines of printing or graphic material from which the alphabetic characters must be distinguished, the data to be read must be identified in some way that is intelligible to the OCR machine. This identification may be as simple as precise placement of the characters on the document or the appearance of a special character at the beginning of readable lines; or it may require a servo-controlled search.

If, however, many lines or a whole page must be read *in toto*, a true 2-dimensional scan is necessary (Fig. 5). The scanner may be fixed, and the documents moved past a read station; difficulties in moving documents have already been discussed. Second, the scanner may move as a unit, going from point to point over a fixed document, presenting both mechanical and interconnection problems. Third, a combination of these is

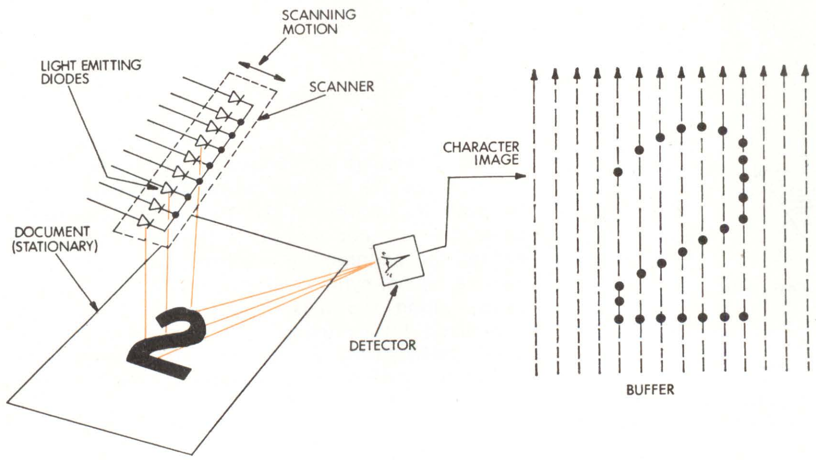

Fig. 4 Multiple light source scanner. One method of scanning documents is to move an array of sources (light-emitting diodes in this example) back and forth across the document, in the X direction, turning on one source at a time to scan at different levels in the Y direction. Output is an image of the character in the buffer

possible, with the scanner moving in the X direction and the document in the Y direction, or vice versa. Fourth, the direction of the optical imaging path may change—an alternative that also presents problems, because optical paths that change direction usually also change length, and therefore must be refocused.

However, at least one optical reader curves the document along a cylindrical arc and deflects the imaging path along the same arc without refocusing it. Another approach is to make the focal length of the optical path very long relative to the degree of deflection, so that focusing changes caused by deflection are negligible. However, this requires either a physically large (but not necessarily heavy) scanner, or a convoluted optical path with many mirrors, prisms, and lenses.

With fiber optics, a fifth alternative becomes possible: a bundle of fibers can be mechanically transported across a document, providing an imaging path of constant length from source to document.

One manufacturer has put a series of self-scanned linear photosensing arrays end to end, with a total length equal to the full width of a page. Documents move past this array, which reads everything in its field across the whole width of the page, in a single sampling. Data are shifted out of the array serially between samples. While this design is imaginative, it is also extremely expensive, compared to alternative ways to use the same technology. Linear arrays cost \$300 per half inch, and this design ties up \$5100 in sensing devices alone in a scanner for 8½-in. wide pages. Whether or not this particular design will be successful in the market depends on future cost reduction in arrays, which may or may not bring the price to a competitive level.

Vacuum-Tube and Solid-State Sensors

The sensor, which is more or less independent from the scanning method, was originally a photomultiplier. However, silicon photosensors, self-scanned arrays, and spectral response modification offer reduced weight and size, TTL compatibility, and a better spectral response, leading to smaller packaging and lower costs; they also contribute to other possibilities such as the mechanical scanning previously mentioned.

Photomultiplier tubes, which respond primarily to ultraviolet light, are also sensitive to visible light that is emitted by paper and ink, some types of which fluoresce under ultraviolet light. This spurious radiation is a source of noise, and papers emitting it were forbidden in old OCR systems. The problem was largely

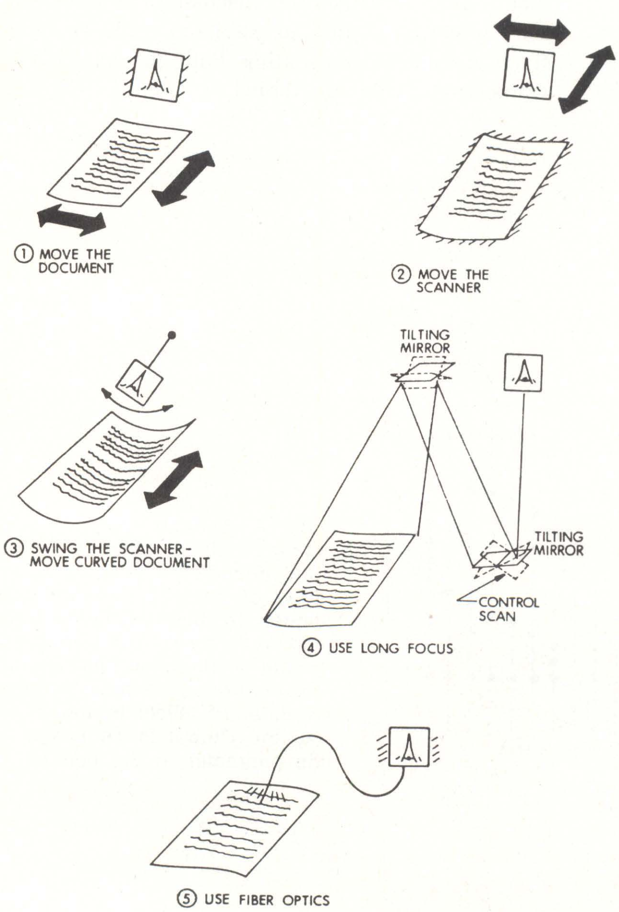

Fig. 5 Scanning techniques. In some machines, the scanner (1) is fixed while documents move beneath it; in others (2) documents are fixed while the scanner moves. A third technique (3) swings the scanner (or a mirror) back and forth over a quasi-cylindrical document that increments along the axis. Focusing problems are minimized (4) by using a long beam path with small deflections. Fiber optics (5) keep both document and scanner motionless, directing light through flexible "pipe"

eliminated by the introduction of silicon photosensors which respond to infrared light. Recent developments in silicon technology have produced photosensors that respond to shorter wavelengths; their spectral response curves are said to be green- and blue-enhanced. These devices, offered by several manufacturers, provide product designers with a much wider choice of characteristics and media interaction.

Photomultiplier tubes are necessarily rather bulky, while silicon photosensors can be closely packed into complex linear and planar imaging arrays, arranged either in a straight line or in a square array. However, silicon photosensors, singly or in arrays, do have disadvantages, some of which have been overcome by recently developed types of vacuum phototubes. Some phototubes, for example, are compatible with solid-state circuitry. In others, new cathode materials offer a much wider selection of spectral wavelength sensitivity than that obtained with silicon technology or the classical photomultiplier. Other advantages include higher resistance in the dark, higher sensitivity and linearity, and long-term stability.

All sensors react to incoming light to an extent that varies with its intensity—that is, they are analog rather than digital. Therefore, their outputs must be converted into digital form—usually with rather low resolution. Four bits provide 16 levels of resolution, which is adequate for most documents. Successive 4-bit units correspond to the black and white areas of the document crossed by a narrow stripe across a character or line of characters swept during a scan. (The reflectance of whole characters varies too little from one to another in samples of equal quality, and too much between samples of different quality, to be reliably recognized as such. A whole character, or a whole line of characters, is therefore assembled during the recognition process from several successive scans across small parts of characters.) These 4-bit units are generally easily distinguishable from one another, unless the document being read is unusually faded or dirty; therefore, they are replaced by 1-bit equivalents. For example, on a perfect document, printed with dense black ink on bright white paper, black may be recorded as 1111 and white as 0000, which are replaced by 1 and 0, respectively. The same document, using faded black ink on old newsprint, might be recorded as 1101 and 0011. Although these numerical equivalents to intensity of reflected light are closer together than in the perfect case, they are also easily distinguishable, and are replaced by 1 and 0. An isolated flyspeck might be picked up in either case, recorded as a dark (1100), and replaced with an isolated 1 in a field of 0's, but the recognition algorithm would ignore it. A problem might arise with a coffee stain, which might show up as an intermediate 0111 amid all the 0000 and 0001 for white paper and the 1101 and 1110 for black ink; the white and the black could be easily classified, but the stain might be put into the wrong class and confuse the algorithm.

From 1000 to 1500 of these successive equivalent bits, obtained from scanning a single character, are stored in a buffer (Fig. 6). A recognition algorithm acts on data in the buffer, transforming them into individual characters in computer code, usually seven or eight bits per character.

Advances in Recognizers

Matrix matching provides the most straightforward method for recognizing characters. Basically, this technique compares an image of an unknown character with a set of idealized patterns, identifying the unknown character with the one pattern to which it corresponds most closely. At one time, optical matching with masked cathode-ray tubes was tried; more recently, idealized patterns have been made with resistor arrays which are faster and can compensate for misalignments more easily.

In such an array, resistors are connected to various stages in a long shift register (Fig. 7) into which the bits of an individual character are shifted from the scanner/digitizer. Certain combinations of bits correspond to individual characters that the system can recognize; when those combinations line up with the corresponding resistors, a current pulse appears in the line corresponding to that character. Smaller pulses appear from time to time in other lines as the bits propagate through the register, but only one pulse is big enough to unequivocally identify the character. The diagram is a vastly simplified representation of such an array, which in a practical system would have several hundred shift register stages, one horizontal line for each character in the set it can recognize, which might number several dozen, and thousands of resistive interconnections—60 to 100 for each character. However, one resistor array must be built for every character in the font to be recognized; consequently, the method is both bulky and costly.

These factors become especially significant in multifont machines—those capable of recognizing characters in any of several fonts—and have stimulated the use of semiconductor memories to store the matrix patterns. Read-only, programmed read-only, and read-mostly memories have all been used this way, maintaining high speed while achieving a new degree of flexibility.

Recognition can be performed in software as well as in hardware. Large general-purpose computing systems have been doing this for many years, working with patterns much more complex than simple alphanumeric characters. Similar techniques are now possible with minicomputers, subject to the drawback of low speed that is intrinsic to software. While many OCR applications are well suited to these speeds, others are being served with hardware-augmented software recognition methods. Such implementations relegate high speed digitization totally to hardware, using software strictly for making decisions.

Some optical character recognition systems now on the market can read a limited set of hand-printed characters—usually the ten decimal digits, a few letters of the alphabet, and some special symbols. Minicomputers offer a potentially cost-effective means to extend the recognizable sets, possibly to all 26 letters, common punctuation marks, and business and technical symbols.

Further decrease in cost can be expected when microprocessors are applied to OCR. Although they are not fast enough yet, they have already shown attractive cost reductions in other applications.

Software techniques and hardware-augmented techniques now available include versions of the fast Fourier transform. These transforms can be processed quickly and inexpensively using currently available hardware subassemblies.

Eventually, character recognition using holographic techniques will be developed. This will represent the closing of a full circle, because it will be a return to the original optical matrix-matching technique. A holographic mask containing a coded "A," for example, used with a laser, could pinpoint the location of all A's on a given document simultaneously. Coordinates of these locations would correspond to memory locations into which A's would be loaded. Then the procedure would be repeated with other masks corresponding to other characters. Whether or not holography can be used with degraded print quality may be the primary technical problem.

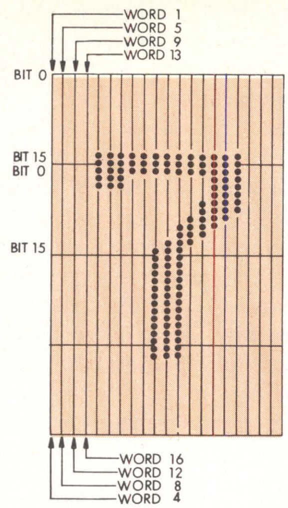

Fig. 6 Scanned character in buffer. After analog sensor output is converted to digital form and then into individual 1's and 0's, the bits are stored in computer words which, if arranged in the proper order and rendered visible, would resemble the original character. This representation is input to the recognition algorithm

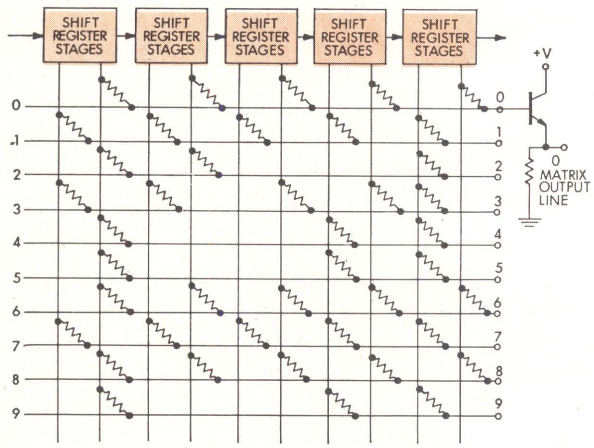

Fig. 7 Resistive recognition. Bits representing an individual character propagate through the shift register (top) in different combinations for different characters. Each bit causes a current pulse in resistors that connect the register stages to the horizontal character lines; for a particular character, the resistors form an adder that accumulates a larger pulse in the line corresponding to that character than in any other line. In practice, the register has hundreds of stages, dozens of character lines, and thousands of resistors

System Integration

Whether holographic techniques or any other technology will find their way into successful commercial machines depends on a total system design approach rather than specific component selection. This approach requires system designers to select a component technology that is consistent with successful integration of the recognition system with its expected environment, including operator interaction, serviceability, and data input and output.

Selecting correct component technologies will not in and of itself guarantee a successful design because many human factors must also be considered. Operators of some previous OCR systems, which had bright flashing lights and laser beams, whirling gears, moving belts, flying paper, and loud bumps and clunks that shook the floor, were best recruited from the engine room of a battleship. Today's system designers might consider packaging their equipment in a physical configuration that resembles card readers or office copiers, to allow operators to use familiar document loading techniques and ordinary stop and go buttons.

High speed applications, such as mail sorting and credit card processing, may well continue with today's physical monstrosities simply because they store documents efficiently after recognition. There are, however, many prospective medium and low speed reading applications that will require reasonably compact devices resembling standard input and output data processing peripherals. A large market exists in business environments for document-to-OCR-to-magnetic tape, where the tape will be processed later at a different location.

For such remote data capture, businesses cannot afford specially qualified operators. A secretary who can operate a Xerox machine should also be able, with equal ease, to perform data entry functions on an OCR machine.

The large numbers of machines that are designed and installed in this new phase will require service from time to time. Inevitably, some of this service will be rendered by less than fully capable service people, or by third party service organizations. Another critical factor is the loss of data entry redundancy that will arise as one OCR machine replaces from five to 12 keypunches; while loss of a single keypunch machine in such an installation only slightly degrades the data entry process, downtime on the OCR machine can stop the whole system.

For these reasons, machines should be designed for maintenance by exchanging modules, and should require no tools, simple tools, or perhaps built-in tools. Furthermore, systems should be capable of self-diagnosis that can isolate the most common failures. OCR designs based on mini- and microcomputers can easily incorporate sophisticated self-diagnosic features at small additional cost.

Similarly, machines must be installable by field personnel rather than factory engineers, without critical alignments; and must permit easy crating for shipment by ordinary transport without sustaining damage to critical parts. These criteria make laser systems less and less desirable.

Throughput, Accuracy, and Error Correction

The only meaningful measure of speed in a character recognition system is the throughput achieved at the output interface. It should be stated in terms of the number of forms output per hour across the interface for a given input quality and kind of document type. This throughput figure has little to do with instantaneous scanning speed or recognition speed, because paper movement generally accounts for a significant fraction of system operating time. In many systems, degraded input copy requires lines or even whole documents to be rescanned, further reducing the throughput. Finally, the size of the document can be critical, as can placement of characters on that document; they affect, respectively, the ease of handling by the mechanism and the time required for the scanner to find the beginning of the data that are to be read.

Although accuracy is a function of the scanning and recognition process, it is measurable only at the output interface, where it can be subjected to real-time correction processes. Quoted reject and substitution rates (proportion of characters not recognized or incorrectly recognized) are virtually meaningless, because they are contingent upon the quality of the input documents. The only meaningful measure of these rates is a sufficiently large sample of real documents run through the machine, followed by an output analysis.

Some currently available machines offer sophisticated error detection and correction techniques. When the machine encounters an unrecognizable character, it can display it on a cathode-ray screen, perhaps with the context. An operator at a console can often figure out what the rejected character should be and enter it through a keyboard. Some systems may stop and wait for such corrections; others store rejected lines on a magnetic tape or disc to wait for more leisurely correction while continuing to process other documents.

Substitution errors in textual input—an occasional misspelled word or even a name—carry enough context to be recoverable, whereas the misrecognition of numbers can cause devastating problems through inaccuracy. Nevertheless, numerical substitutions can be recovered through a few simple techniques. Check digits, for example, can be used with serial numbers, part numbers, invoice numbers, or similar input, and verified by the machine. Forming part of the number, the check digit is related to the other digits by an explicit formula. Other numbers, such as prices on an invoice, cannot have check digits, but can be checked for accuracy by arithmetic techniques. For example, an invoice ordinarily lists both the prices for the individual items and the total bill; individual prices as read by the OCR system can easily be added up and compared with the total as read. If the recognized sum and the internally computed sum are different, a substitution can be presumed somewhere along the line. For both types of numbers, the substitution is detected, but not corrected. It can only alert the operator or the system that an error has occurred.

Scanner resolution also affects accuracy. A recognizer working from digitized characters in a 7 x 9 matrix, over the long run, will give considerably different results from a similar recognizer working with a 20 x 32 matrix. Here again, accuracy or departure from accuracy manifests itself at the output interface.

Input Is Important

The data input interface is more important than it may seem. Customers buy optical character recognition systems to serve as tools in processing important documents. They are interested in the scannable documents, not in the machine that processes them. A corollary to this is that an OCR system, whenever possible, must process existing forms in their present formats and on their present paper stock, using the same ink. Trying to sell a customer a system that works only with redesigned forms is almost sure to fail.

On the other hand, selling the customer a system with the assurance that it will work with his present forms, when in fact it would work better with redesigned forms, is likely to create ill will. His forms may contain data that the machine should ignore, or preprinted information that it should pick up along with variable data printed in a different ink. With OCR registration (accurate placement) of printed data can be important. With such considerations as these in mind, forms redesign could make the difference between success and failure.

At least two machines now on the market can describe the format of a scannable document and differentiate scannable from nonscannable areas in a flexible manner.

Rapid technological advances in the computer and peripheral industry can make a machine purchased today obsolete tomorrow. To combat obsolesence, an OCR system's fixed mechanical and electronic components can be built with general-purpose control capability, with readily alterable operational characteristics stored in memories, floppy discs, or other interchangeable media, so that the user can upgrade his system at minimum cost. Such machines are most flexible when controlled by a minicomputer or microprocessor. At least one machine now on the market maintains all its operational characteristics on a single floppy-disc cartridge—including recognition font algorithms as well as the document processing and scanning control systems. As new fonts or more sophisticated error-correction techniques become available, this machine's users will benefit from them without replacing the machine.

Richard K. Dove holds a BSEE degree from Carnegie-Mellon University, Currently director of marketing at Ball Computer Products, where he is responsible for three product lines, his background includes experience in systems programming and in systems analysis.

DESIGN NOTE

Index-Register Logic Saves One Instruction per Loop

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Army Electronics Command
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Two added registers and a few gates eliminate a decrementing instruction from a loop, thus increasing a program's speed under some conditions

Index registers—an important subsystem in any modern digital computer—contribute to easy programming and fast execution of repeated subroutines (loops), by simplifying address modification through added logic hardware. Even greater speed of indexed loops is possible if the programmed instruction that increments or decrements the index register is eliminated,* through use of additional hardware. It can save one instruction per loop.

If the number of instructions in a loop is small and the number of times the loop is executed is large, the modification may save a sufficient amount of computer time to warrant the cost of the extra hardware. The modification is clearly application dependent; it could pay off handsomely in some dedicated systems, and not pay off at all in others.

For example, a simple loop can consist of four instructions—in memory locations A_1, A_2, A_3, and A_4—that are to be repeated in sequence a predetermined number (N) of times. Initially, an index register (XR) is loaded with the number N. Suppose the fourth instruction in the loop decrements the XR by 1 and tests to see if the XR contains 0. If it does, the program exits from the loop and executes the instruction at the next address, A_5; but if the XR does not contain 0, the program returns to the instruction at A_1 for another iteration, address A_1 being specified as an operand address of the instruction in A_4. Many computers contain index-register logic that works in essentially this way.

The programmed instruction in A_4 can be eliminated by adding extra registers and logic. One new register, called the index address (IA) register, is loaded with address A_3 before beginning the first iteration of the loop (just before or just after loading N into the XR). A second new register, called the loop address

*D. Mandelbaum, "On Parallel-Acting Index Registers," *IEEE Transactions on Computers*, Mar 1971, p 361

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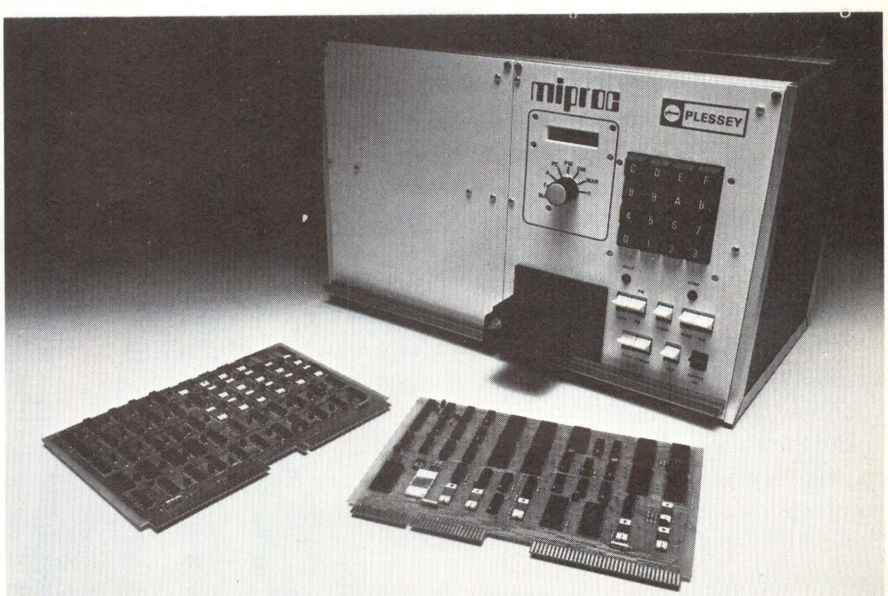

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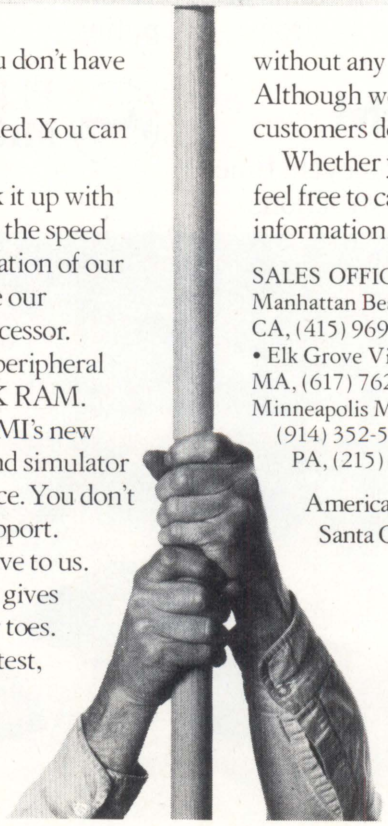

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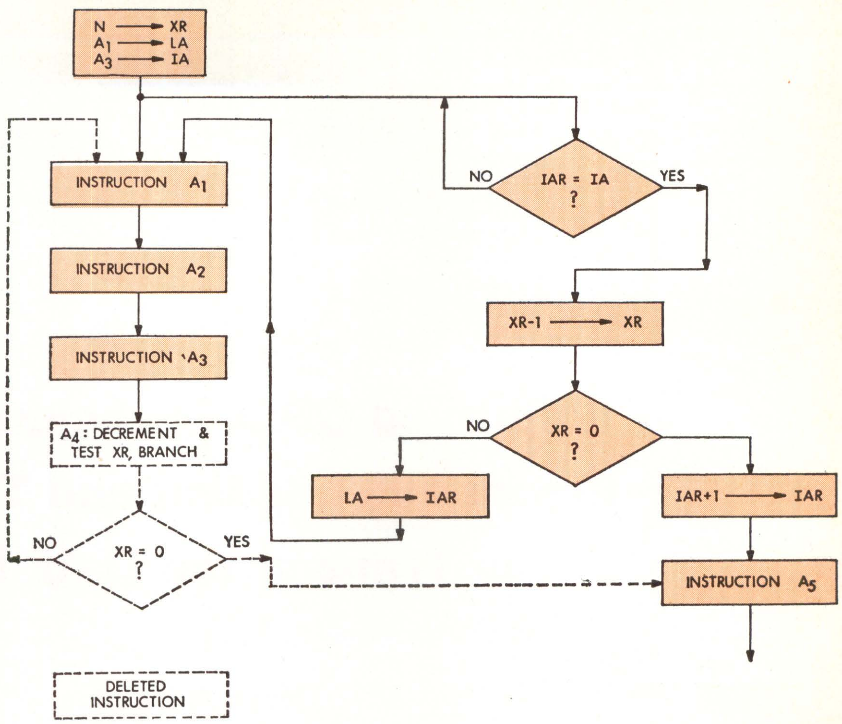

Parallel comparison. When the last instruction in the shortened loop is fetched, equality of the contents of index-address (IA) and instruction-address (IAR) registers decrements the index register (XR), which forces another pass through the loop, unless it has been decremented to 0

(LA) register, is loaded with address A_1, also before executing any part of the loop (see Figure).

When the processor fetches the instruction in A_3, the contents of its instruction address register (IAR) match those of the IA register; the equality condition is a signal to decrement the XR. If this makes 0 appear in the XR, the computer's next instruction is in location A_5 (the IAR is incremented normally and A_4 has been deleted); but if the XR is not yet 0, LA register contents are transferred to the IAR, so that the next instruction again becomes the first instruction in the loop.

Two additional registers (IA and LA) and associated gates are required, together with simple arithmetic logic for decrementing the XR. In some computers, the main arithmetic unit is used for this decrementing; but if that unit is in use while the last instruction in the loop is being executed, a separate decrementer is necessary.

A similar modification that is more generalized requires a third added register (RA) in addition to the IA and LA registers. The RA is set with a specified number before beginning the loop. Then, when the contents of the IA and LA registers match, XR's contents are compared with those of the RA, and the program is made to branch or not branch, depending on the match. Special instructions in the program before the loop is entered specify what happens at this point. Another modification can specify that the XR be incremented or decremented by steps greater than 1.

These additional instructions are executed only once, before the loop is started; they save one instruction per loop, which otherwise would be executed many times and detract significantly from the computer's operating speed. □

TECH NOTE

Improved CRC Technique Detects Erroneous Leading and Trailing 0's in Transmitted Data Blocks

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Bedford, Massachusetts

New bit-oriented data communication protocols using conventional CRC error-detection methods can fail when presented with erroneous leading or trailing 0-bits. A simple artifice overcomes this deficiency

Conventional error detection procedures with cyclic redundancy check (CRC) codes fail to detect erroneous leading or trailing 0-bits because, when the shift register implementing the code reaches an all-0's state, any number of additional 0's can be shifted into it without changing its state. A solution to this problem is, first, to set the register initially to all-1's instead of all-0's, and second, to invert (ie, complement) the CRC check bits that follow each transmitted block of data.

This solution, developed by IBM, is being incorporated by the American National Standards Institute (ANSI) into its proposed Advanced Data Communication Control Procedures (ADCCP[1]), presently being developed by Task Group 4 of ANSI X3S3. (Committee X3 develops standards related to computer technology, and subcommittee S3 is concerned with digital data transmission between computers and related equipment.) This article provides the rationale for the new procedure and, in doing so, presents some elementary concepts concerning error detection, shift registers, and link control procedures.

Background

CRC error detection involves polynomial division using modulo-2 addition, equivalent to the exclusive-OR logic function. The procedure will be illustrated with a specific example; a more formal and rigorous discussion can be found in the classic paper by Peterson and Brown.[2]

In order to transmit the eight data bits 11101100 with detection of errors arising during transmission, five check bits are appended. To determine what these five bits are, five 0's are appended to the data bits and the string of 13 bits is divided modulo 2 by a divisor of six bits (ie, a fifth-order polynomial). In general, the division will not "come out even"; there will be a remainder which replaces the five added 0's. Choosing 100101 (ie, $x^5 + x^2 + 1$) for the divisor, the operation and its results are

$$\frac{1110110000000}{100101} = 11110101 + \frac{00001}{100101}$$

Adding the remainder 00001 to the data bits, the transmitted string becomes 1110110000001.

In mathematical terms, the data bits to be transmitted are represented by the polynomial

$$\begin{aligned} D(x) &= 1 \cdot x^7 + 1 \cdot x^6 + 1 \cdot x^5 + 0 \cdot x^4 \\ &\quad + 1 \cdot x^3 + 1 \cdot x^2 + 0 \cdot x^1 + 0 \cdot x^0 \\ &= x^7 + x^6 + x^5 + x^3 + x^2 \end{aligned}$$

Adding the five 0's is equivalent to multiplying this polynomial by x^5, and the divisor corresponds to another polynomial, $P(x)$, whose order

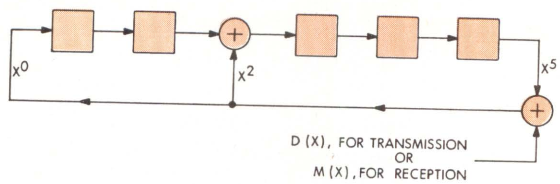

Fig. 1 Linear feedback shift register. When a data block to be transmitted—viewed as polynomial D(x) or message M(x) as received—passes through this shift register, it is effectively divided by the polynomial $P(x) = x^5 + x^2 + 1$, producing either a string of redundant check bits for the end of a message, or an indication of errors picked up during the message transmission

is the same as the number of check bits. The division is

$$\frac{x^5 \cdot D(x)}{P(x)} = Q(x) + \frac{R(x)}{P(x)}$$

Replacing the five added 0's with the five bits of the remainder creates a new polynomial, M(x), the message that is actually transmitted:

$$M(x) = x^5 \cdot D(x) + R(x)$$

$$= 1110110000001$$

When M(x) is constructed in this manner, it is guaranteed to be evenly divisible by P(x) at the receiver, if no errors have been picked up in the communication channel. If, following the same division process at the receiver, $R(x) \neq 0$, M(x) as received is known to contain one or more errors. (CRC error detection provides no information on the location or number of errors.) If $R(x) = 0$, we conclude that either no errors have occurred or an error has occurred which is undetectable.

Any number of 0-bits may precede or trail M(x) and, when the division process is completed, the remainder will still equal 0. Thus the conventional CRC error detection procedure will not, by itself, detect the presence of erroneous leading or trailing 0-bits.

Choosing the number of check bits, selecting a polynomial, and evaluating the probability of an undetected error is a rather esoteric art. The decisions are based strongly on maximum length of the data block to be transmitted, probability distribution of channel errors, highest probability of undetected error that is acceptable to the user, and efficiency (ratio of data bits to data bits plus check bits) with which the channel is to be operated.

TABLE 1

Shift Register States in Simple CRC

	Shift Register	Transmitted Bits		
Initial state →	00000			
	10100	1	D(x)	M(x)
	11110	1	D(x)	M(x)
	11011	1	D(x)	M(x)
	11001	0	D(x)	M(x)
	01100	1	D(x)	M(x)
	10010	1	D(x)	M(x)
	01001	0	D(x)	M(x)
Transmitted by sender →	10000	0	D(x)	M(x)
	01000	0	CRC bits	M(x)
	00100	0	CRC bits	M(x)
	00010	0	CRC bits	M(x)
	00001	0	CRC bits	M(x)
Final state at receiver →	00000	1	CRC bits	M(x)

Linear Feedback Shift Registers

Linear feedback shift registers in CRC calculation perform polynomial division with modulo-2 addition using simple components. The shift register shown in Fig. 1 performs the calculations for the preceding example; its successive states are shown in Table 1.

The procedure begins by setting the initial state of the register to 0. After the last bit of D(x) has been shifted into the register, its contents are the CRC bits, the same as the remainder calculated in the example. They would be shifted out of the register and into the communications channel at the transmitter. At the receiver, the identical division process is performed on M(x). In the absence of channel errors, the final state of the register, as shown, will be 0.

Link Control

Starting and stopping the CRC computation are typically determined by the link controller, usually a device connected to a processor's I/O bus. It controls the line equipment (eg, a modem) and performs conversions between the parallel data format of the I/O bus and the serial

SYN , STX,. . . DATA CHARACTERS . . . , ETX , CRC , CRC

Fig. 2 Character-oriented data block. Synchronizing characters (SYN) precede the block; start-of-text (STX) signals its beginning and end-of-text (ETX) indicates its end, just before the CRC bits arrive

OPENING FLAG SEQUENCE — CLOSING FLAG SEQUENCE

F, . . . DATA BITS . . . , FCS, F

F = FLAG SEQUENCE = 01111110
FCS = FRAME CHECK SEQUENCE (16 CRC BITS)

Fig. 3 Bit-oriented data block. As proposed for ADCCP, this format permits any arbitrary sequence of bits in the data block

data format of a communications channel.

Most synchronous data communications circuits perform link control functions through the use of control characters in the American Standard Code for Information Interchange (ASCII). A typical character-oriented link control procedure is IBM's Binary Synchronous Communications (BSC) protocol. In this procedure, ASCII control characters STX and ETX delimit a block of data (Fig. 2). Control characters consist of seven ASCII bits plus one parity bit:

SYN—(Synchronization) (0010110). One or more precede every data block and are used by the link controller to establish character framing

STX—(Start-of-Text) (0000010). Indicates beginning of data block; used by the controller to determine when to begin the CRC computation

ETX—(End-of-Text) (0000011). Indicates end of data block; its arrival at the link controller signals that the next two characters constitute 16 CRC bits, and tells the link controller to stop the CRC computation

Link controllers using the BSC protocol have no difficulty detecting erroneous leading or trailing 0's. The reason, however, has nothing to do with the CRC computation; rather, it is because *specific* nonzero control characters are used to delimit a data block. Thus, for example, if the STX character that immediately precedes the data characters is erroneously changed to all 0's, the link controller will refuse to accept it as a valid block delimiter.

No such restriction applies to ADCCP, which is a bit-oriented, rather than character-oriented, link protocol—as are IBM's recently announced Synchronous Data Link Control (SDLC) and the High-Level Data Link Control (HDLC) of the International Standards Organization (ISO). A data block in ADCCP is called a frame (Fig. 3). Flag sequences, which combine the functions served by STX, ETX, and SYN in BSC, delimit the frame and establish character synchronization.

Unlike BSC, ADCCP places no restrictions on any of the data bits. Any combination of bits can be used anywhere in a message; yet ADCCP will be transparent to it. Transparency is achieved through the use of a 0-bit insertion/extraction technique.

The transmitter inserts a 0-bit following five consecutive 1-bits anywhere between the beginning and ending flag of the frame. The receiver continuously monitors the received bit stream. When five contiguous 1-bits are received, the sixth bit is inspected: if it is a 0-bit, it is discarded: if it is a 1-bit, the seventh bit is inspected. If the seventh bit is 0, a flag sequence has been received: if it is 1, an abort sequence has been received. As seen on the transmission link, 0-bit insertion may increase the length of a frame by as much as 20%. For example, if 100 consecutive 1-bits were to be transmitted, a total of 120 bits would actually be sent (100 1-bits plus a 0-bit inserted after every fifth 1-bit).

The Problem

In ADCCP, as in BSC, conventional CRC computations will fail to detect erroneous leading or trailing 0-bits. Unlike BSC, however, ADCCP has no means of distinguishing between false starts and true starts. CRC computation begins with the first non-flag character, rather than a specific control character, and continues until a closing flag is detected. As a result, if channel errors change the opening flag to all 0-bits, these bits will not change the state of the register, which has been initialized to 0. The error will not be detected. Similarly

TABLE 2

Shift Register States in Revised ADCCP

	Shift Register	Transmitted Bits	Span	
Nonzero initial state →	11111			
	01111	1	D(x)	M(x)
	00111	1	D(x)	M(x)
	00011	1	D(x)	M(x)
	10101	0	D(x)	M(x)
	01010	1	D(x)	M(x)
	10001	1	D(x)	M(x)
	11100	0	D(x)	M(x)
These CRC bits are complemented before transmission →	01110	0	D(x)	M(x)
	10010	1	Inverted CRC bits	M(x)
	11101	0	Inverted CRC bits	M(x)
	11010	0	Inverted CRC bits	M(x)
	01101	0	Inverted CRC bits	M(x)
Unique nonzero final state →	00110	1	Inverted CRC bits	M(x)

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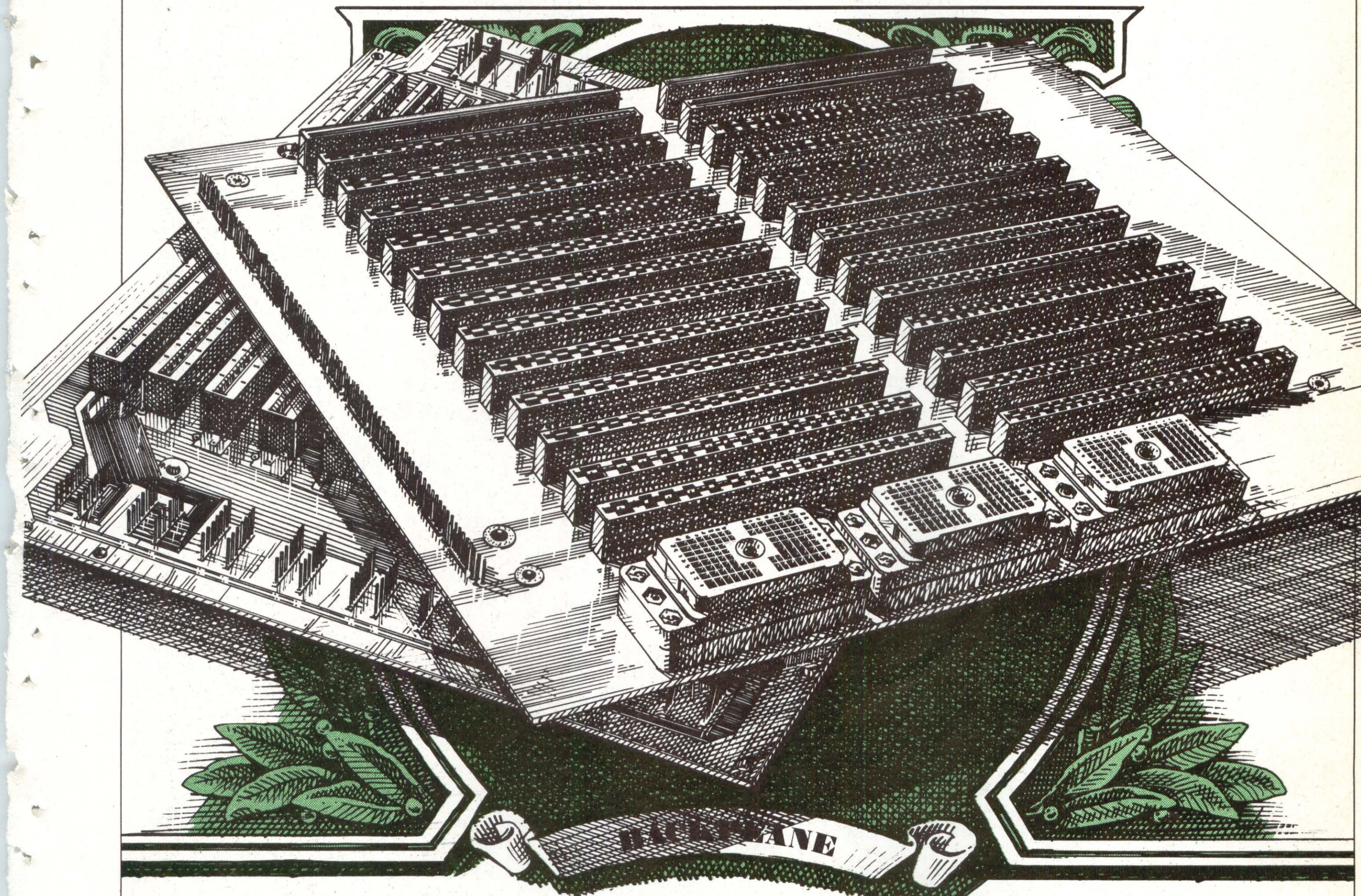

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if channel errors change the closing flag to all 0-bits, when the last CRC bit is shifted into the register it will reach an all-0 state. The erroneous trailing 0-bits will not change the state of the register, and thus will not be detected.

The Solution

Non-detection of erroneous leading 0's occurs because the shift register is set to 0 before beginning a CRC computation. The solution, which is somewhat obvious, is to initialize the shift register to any nonzero value. Leading 0's will then change the state of the register and be detected. In ADCCP, the register is set to all 1's.

Non-detection of erroneous trailing 0's occurs because, in the absence of channel errors, the shift register reaches an all-0 state. Initializing the register to a nonzero value is no help. The division process will still come out even, and the remainder will be 0. The solution, which is not obvious at all, is to transmit the 1's complement of the CRC bits. In terms of the example, after D(x) has been transmitted, each CRC bit is complemented (inverted) prior to transmission. This technique causes the receiving shift register to reach a unique nonzero state. Trailing 0's will then change the state and be detected. This technique is illustrated in Table 2.

There is more than one method of achieving a solution that is functionally identical to the one described above. With respect to the example shown in Table 2, rather than presetting the 5-bit shift register to an all-1 state, the first five data bits may be inverted prior to entry into the shift register. Starting with an all-0 register state and inverting the first five data bits is functionally identical to starting with an all-1 state and not inverting the first five bits. (A mathematical description of the alternative design approaches is provided in Ref. 1, which may be obtained from CBEMA, 1828 L St NW, Washington, DC 20036.)

Reference

1. ANSI Document X3S34/589, Proposed American National Standard for Advanced Data Communication Control Procedures
2. W. W. Peterson and D. T. Brown, "Cyclic Codes for Error Detection," *Proceedings of the IRE*, Jan 1961, pp 228-235

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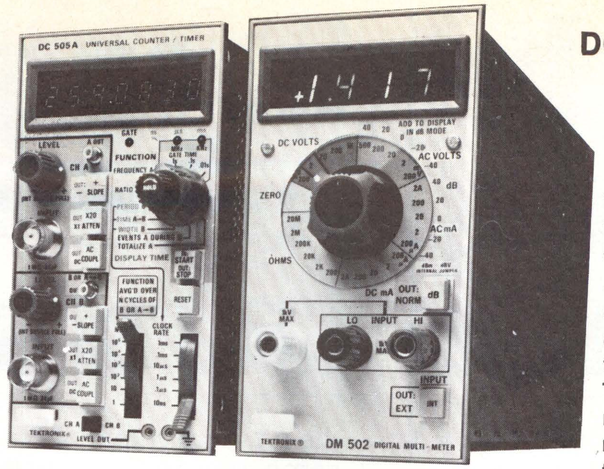

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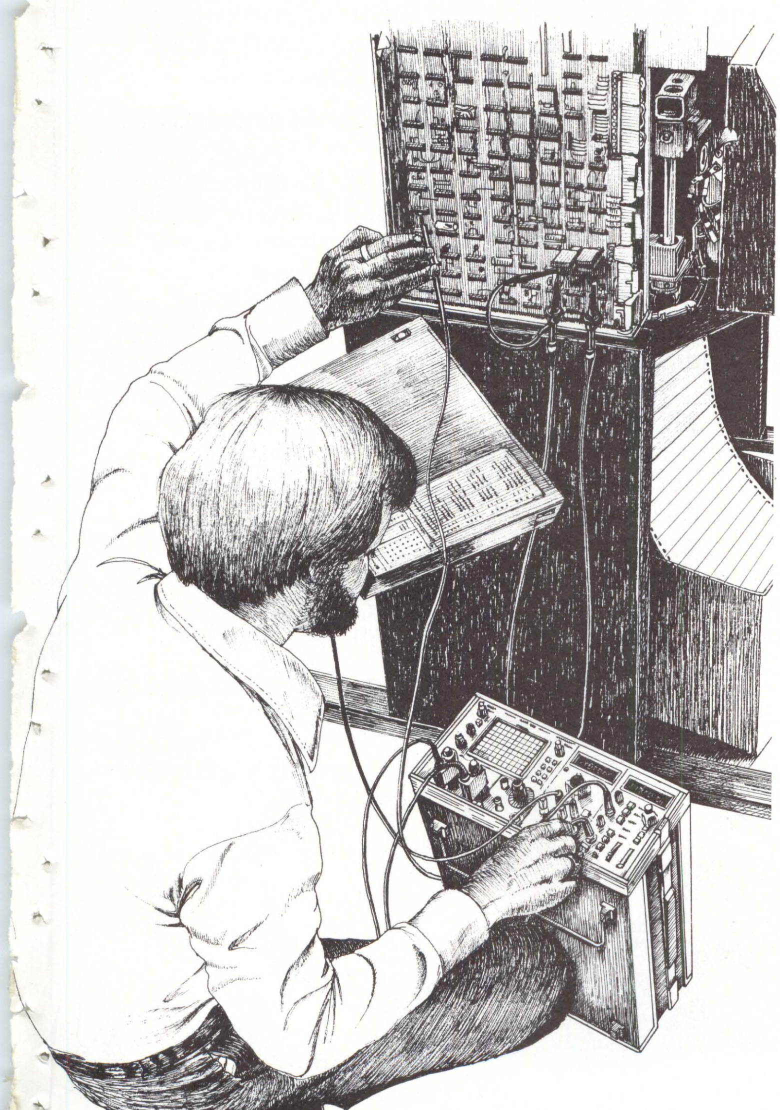

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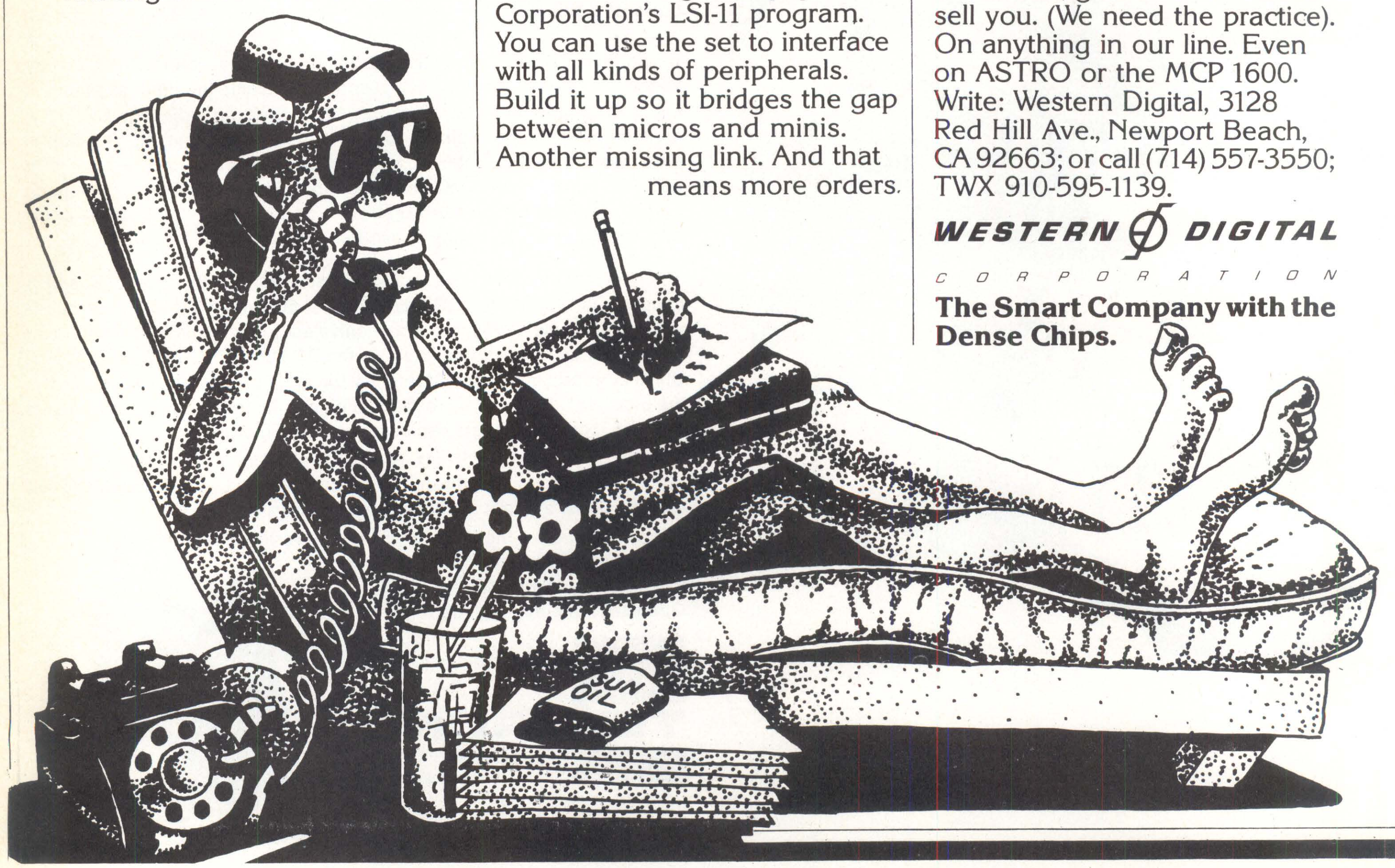

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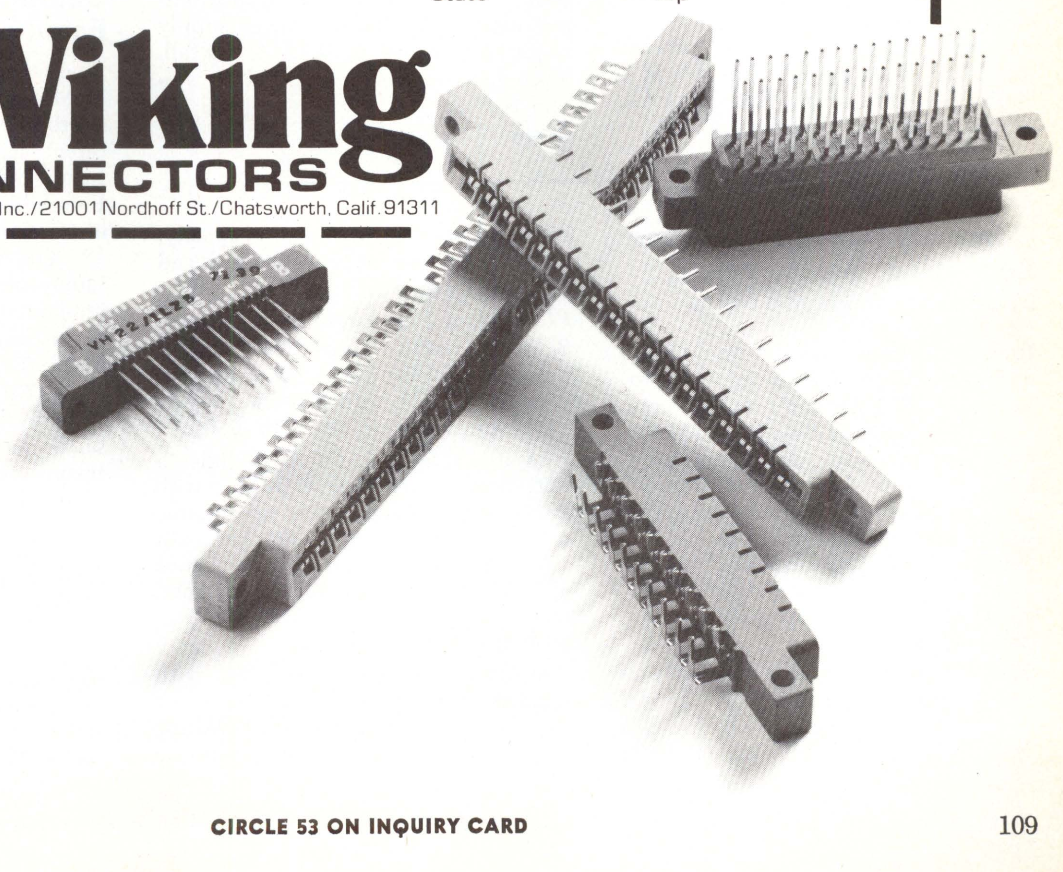
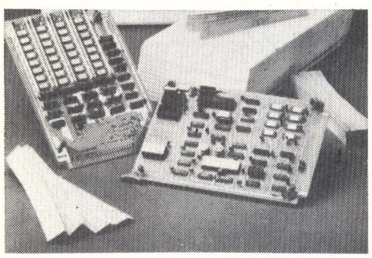


CIRCLE 53 ON INQUIRY CARD

System Teaches User How To Design Micro-Processor-Based Products

A microcomputer system that serves both users who want to design their own microprocessor-based products and those who simply want to learn about microprocessor concepts has been announced by Mostek Corp, 13300 Branch View Lane, Dallas, TX 75234. The general evaluation microprocessor system (GEMS-8) can function in applications such as test/instrumentation, data terminals, POS



terminals, communications, industrial control, education, medical instrumentation, or traffic light controllers by adding teleprinter interface, cabinet, and power supplies.

Each system is made up of processor board designed around the MK 5065, 8-bit microprocessor; a PAR (Programmer Aid Routine) ROM to aid in development of specific application programs; and a 12K x 8 memory board with direct interface to the processor board. Software support includes a resident assembler which can generate object tapes from source tapes, an ASCII dump, which dumps memory in ASCII format, and a text editor for generating and modifying the source text prior to assembly. Documentation is provided through a system manual with detailed descriptions of hardware, programs, and applications.

The processor board has a universal I/O port, TTL-compatible variable baud rate, and 51 basic instructions with a typical execution time of 7 μs, and addresses a 32K x 8 memory space with 1K RAM located on the board. Triple-level architecture allows rapid interrupt servicing. The PAR ROM contains a standard loader and allows initialization of internal registers including the stack pointer, execution of the standard loader, writing and dumping of memory data, execution of user programs, and breakpoint operation. The memory board features totally transparent automatic refresh and separate address, data input, and data output buses. Both data input and data output can be wire-ORed. Power supply requirements are 5, ±12 V for all. Price for the complete GEMS-8 system is $995.

Circle 170 on Inquiry Card

Company Announces Price Reductions on Micro-Processors/Computers

Price reductions ranging from 16 to 23% have been announced by Pro-Log Corp, 852 Airport Rd, Monterey, CA 93940 on its PLS-400 series 4000, 4-bit logic processor systems and MPS-800 series 8008, 8-bit microcomputers. Both series couple the microprocessor with memory, clock, and flexible I/O circuitry for use in dedicated control and data processing. Crystal-clock circuits, previously an extra-cost option, are now standard.

PLS-401, a 1-card system, includes an Intel 4004 microprocessor, crystal clock, 256-word instruction p/ROM with 1024-word capacity, 80-char data RAM with 320-char capacity, and external power-on reset; reduced from $355 to $295.

PLS-402, a 2-card system, includes a 256-word instruction p/ROM with capacity to 1536 words, and an 80-char data RAM with 320-char capacity; reduced from $470 to $395.

PLS-403, a 3-card system, includes a 256-word instruction p/ROM with 2560-word capacity card expandable to 4096 words, and an 80-char data RAM with 640-char capacity card (expandable to 1280 char); reduced from $590 to $470.

PLS-411, a 1-card system, includes a 256-word instruction p/ROM with capacity to 768 words, a socket for the Intel 8316 2048-word ROM or for a ROM simulator card, and an 80-char RAM with 560-char capacity; reduced from $420 to $320.

(-401 and -411 have 16 TTL input and 16 TTL output lines; -402 and -403 have 32 field-selectable TTL I/O lines, card-expandable to 128. All have four MOS output lines.)

MPS-803, a 3-card system, includes a 256-word instruction p/ROM with 1024-word capacity, and a 1024-word program or data RAM with 2048-word capacity; has 28 TTL I/O lines, field-selectable in groups of four as input gates or output latches; reduced from $810 to $620.

MPS-805, a 5-card system, includes a 256-word instruction p/ROM with 2048-word capacity, and a 1023-word program or data RAM with 4096-word capacity p/ROM or RAM card expandable to 16,384 words; has 32 TTL output latches and 32 TTL input gates; I/O is card-expandable to 192 output latches and to 64 input gates; reduced from $980 to $790.

Circle 171 on Inquiry Card

First of Software-Compatible μProcessor Family Announced

Plug-compatible with the bus system of Motorola's MC6800, the MCS6501 microprocessor has the ready and indirect memory access capability of Intel's 8080 and the on-chip clock of Fairchild's F-8. In addition, it uses instruction sets based on DEC's PDP-11. The 8-bit device is the first of a family of n-channel, silicon-gate, ion-implanted, depletion-load microcomputer components to be announced by MOS Technology, Inc, 950 Rittenhouse Rd, Norristown, PA 19401. Although the present device uses the same clock structure as the MC6800, future versions will not have that limitation.

In addition to other members of the software-compatible microprocessor family, future announcements will include both compatible and advanced I/O devices, ROMs, and RAMs, based on MC6800 bus architecture which the company feels will become an industry standard. The MCS6501 will sell for under $20.

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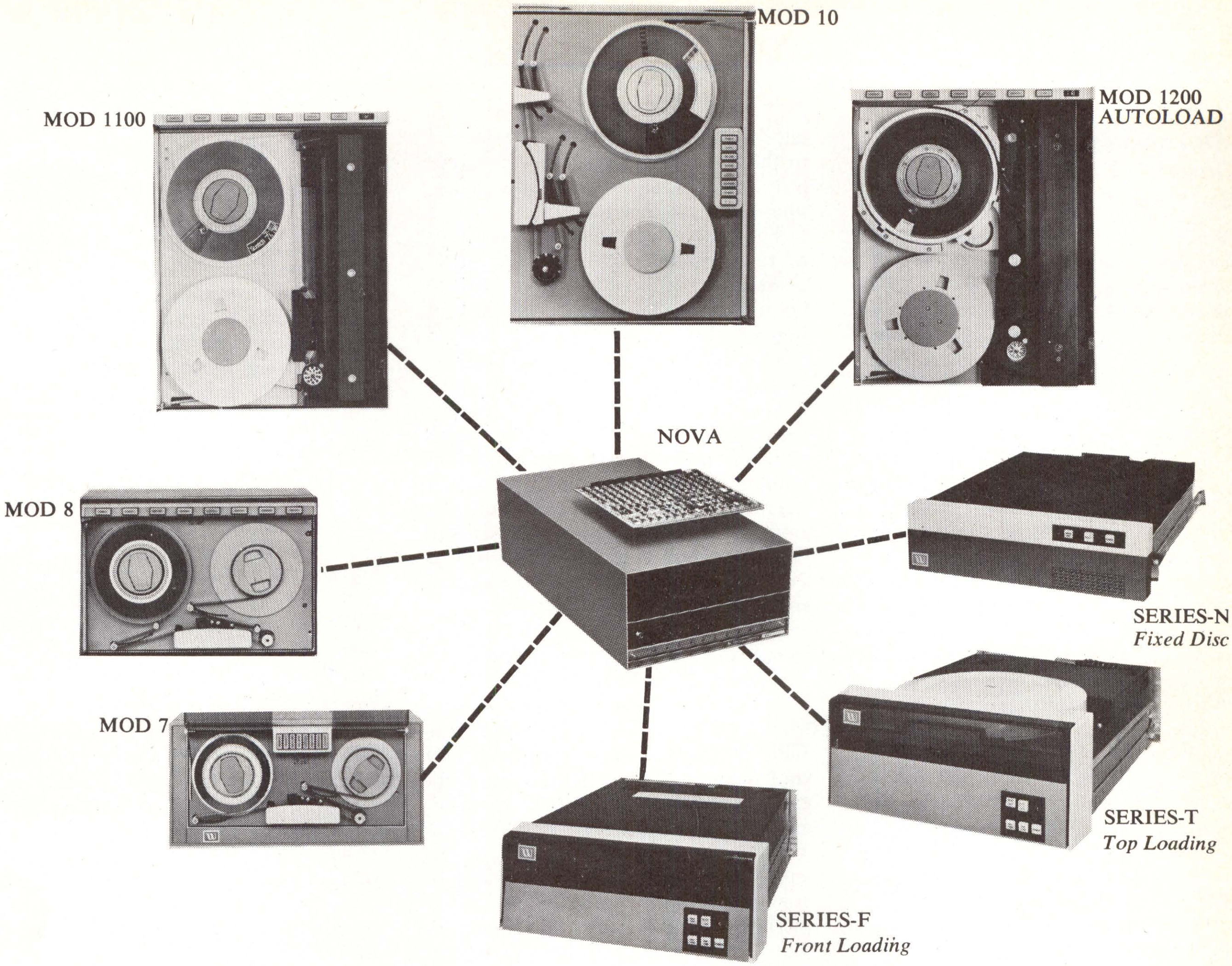

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Microcomputer System Capabilities Enhanced By Added Components

A number of additional components, including a higher performance CPU, which enhance the company's 8080-based MCS-80™ microcomputer system have been announced by Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051. Included are an 8080A CPU, with four options; two LSI CPU group components; and five programmable I/O and peripheral devices.

The 8080A CPU is a single-chip, 8-bit parallel unit (byte processor) fabricated with silicon-gate, n-channel MOS technology, and is completely interchangeable with the 8080. Whereas the 8080 operated with a 2-μs instruction cycle over the commercial temperature range, the 8080A can operate at that speed over the military temperature range (M8080A) and at 1.3 μs over the commercial range (8080A-1), providing up to 35% more throughput than other n-MOS microcomputers. Two other options are available: operation at 1.5 μs/cycle (-2) and 2 μs/cycle (standard 8080A), both over the commercial temperature range.

Full TTL drive on all outputs (1.9 mA at TTL levels) enables the CPU to drive p/ROM, ROM, and RAM systems directly. In addition, it provides direct interface to TTL or MOS I/O devices. Logic improvements can be used to simplify direct memory access (DMA) operations in smaller systems and interrupt control in larger systems. Because the program counter is not incremented for each byte of the instruction, a multi-byte instruction can be used as an interrupt vector. This facilitates control of more than eight interrupt levels. The use of vector information for interrupt definition allows a virtually unlimited number of priority interrupt levels to be processed by an 8080A-based system.

Functions which normally would require the addition of 10 to 15 TTL packages and a variety of discrete components for timing, bus control, buffer, interface, and other functions have been combined in the two CPU group components. A standardized bus structure permits all present and future MCS-80 components to be attached directly in building-block fashion. The group makes all CPU inputs asynchronous in nature, allowing other components to be attached to the bus without timing or interface problems. In addition, system noise immunity is increased.

The 8224 clock generator includes a tank circuit that allows either overtone or fundamental crystals to be used, so that stable system timing can be achieved at any desired clock rate. Among the extra functions provided are TTL clock output, which is synchronized with MOS clock outputs; auxiliary timing functions, which can be used to establish communications baud rates, delays, or gating operations during DMA activities; and built-in control of power-on reset and "ready" synchronization (as well as control of single-step operation, often required in development work).

The 8228 system controller replaces latches, TTL gates, and buffers normally added to a CPU to isolate bus sections and attain asynchronous bus control. It latches the CPU status and then generates I/O and memory control signals. In addition, it provides a built-in dual bidirectional bus driver operating at bipolar drive levels, providing the current-sinking capability required for simple interfacing of the CPU with I/O and memory devices; isolation of the data bus by the driver, allowing memory bus timing to be optimized independently and relaxing memory speed requirements; and built-in single-level interrupt vector.

Programmable in the system with software rather than at the time of manufacture, programmable I/O and peripheral devices enable operating modes to be changed dynamically during system operation. Variety of building blocks per system is minimized, allowing the equipment manufacturer to use a basic component set or microcomputer assembly for a wide variety of equipment models. The devices, all silicon-gate, n-channel MOS LSI, are:

8251 programmable communications interface, a software-reconfigurable universal synchronous-asynchronous receiver/transmitter (USART) interfacing with serial data communications lines, implements virtually all serial communications protocols in use today, including IBM Bi-Sync, under program control. Unlike conventional USARTS, it does not require supplementary posts, logic, or bus interfaces. Character length is variable from 5 bits to a full 8-bit byte. Clock rate is variable. Asynchronous baud rates are dc to 9.6 kilobaud, and synchronous baud rates are dc to 56 kilobaud. In synchronous mode, sync character insertion is automatic.

8255 programmable peripheral interface provides three multipurpose, 8-bit I/O ports. The 24 I/O lines can be combined in various software-organized configurations to interface peripheral devices. Built-in bit-set and -reset functions reduce the amount of software required to change control words in external equipment. High current output is provided for driving long lines, Darlington-type drivers, and displays.

8253 programmable interval timer provides software-variable control of system timing functions, and generates such timing signals as baud rates, as well as time-out delays for motors and timing for peripherals. Three independent 16-bit counters allow the timer to simultaneously track three independent events. The device counts at dc to 3 MHz, as well as in binary or BCD, eliminating conventional binary-to-BCD conversions and conversion software.

8257 programmable DMA controller interfaces bulk storage devices, and can provide DMA to multi-drive memories. It features four prioritized channels of DMA request logic, simplifies use of system DMA/hold functions, and allows these functions to be "hidden" in the CPU execution cycle. The resulting increase in data transfer rate allows more efficient use of RAM. All channels provide modulo 128 and terminal count flags for disc sectoring and "transfer complete" indication.

8259 programmable interrupt controller allows the system's response to interrupts to be varied dynamically. It simplifies interrupt control, increasing system response speed. In addition, it simplifies programming and allows interrupt priorities to be varied "on the fly" whenever equipment operating requirements change. It controls eight interrupt levels per device, and can be expanded to control 64 levels with eight controllers. Vector "anywhere" operation eases programming. Simple call instructions are inserted as vectors, enabling any interrupt processing routine to be selected.

All devices listed are available from stock, with the exception of the 8253, 8257, and 8259, which will be available late this year. The 8080A is supplied in a standard 40-pin DIP; all others are provided in standard 16-, 28-, or 40-pin DIPs.

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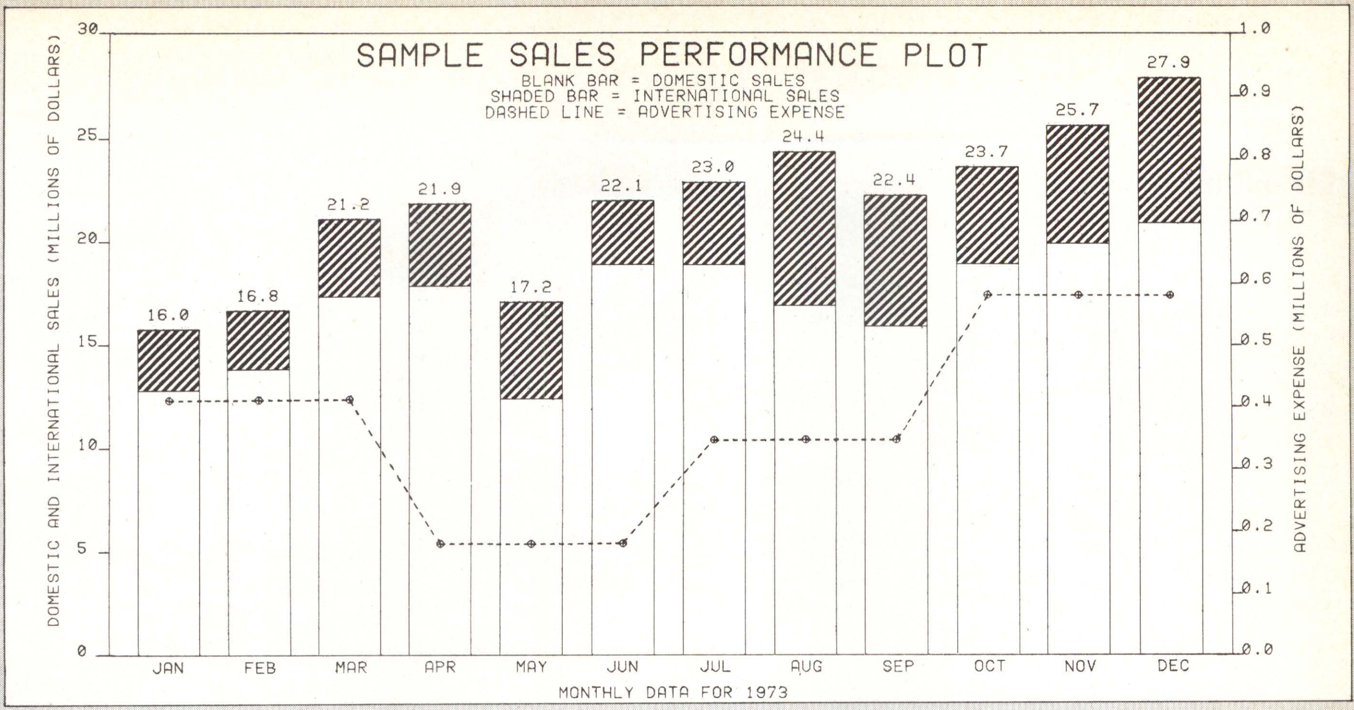

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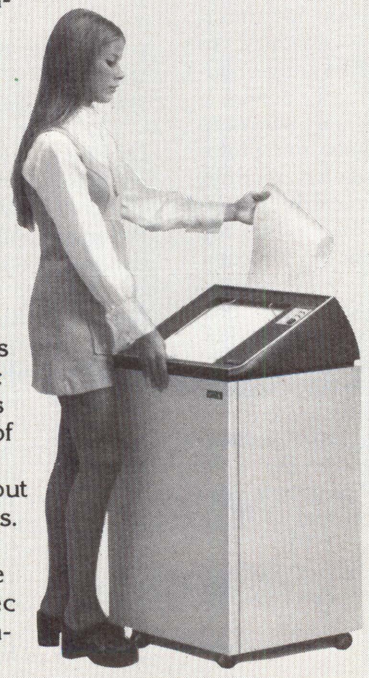

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CIRCLE 55 ON INQUIRY CARD

Support Product Aids in Development of M6800-Based Systems

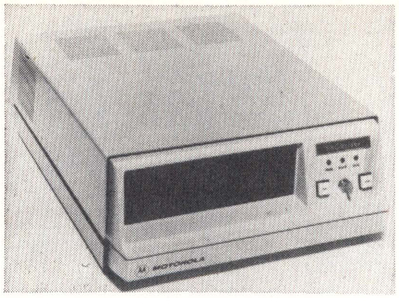
First in a series of support products designed for the M6800 microcomputer, the EXORciser™ development aid for microcomputer-based systems incorporates hardware/software elements of the 6800 family. It can emulate a 6800-based design in real time or can be configured to simulate other logic approaches. The instrument is being built in a facility dedicated by Motorola Semiconductor Products Inc, PO Box 20912, Phoenix, AZ 85036 solely for the manufacture of 6800-related products.

Basically, the instrument is made up of three plug-in logic modules (cards) and a power supply within a standard 19" wide chassis that is available in either rack-mountable or table-top versions. A printed-circuit "mother board" in the bottom of the chassis provides signal and power distribution among 14 sockets; two sockets are reserved for two of the basic modules, and the remaining 12 allow for expansion of the configuration. Optionally offered or customer-designed memory, I/O, or special-function cards inserted into the 12 expansion locations have access to both the EXORciser power bus and the M6800 system bus.

One basic module, the MPU, contains an MC6800 microprocessor; a 2-phase clock generator that can be controlled by an external source or an internal 1-MHz crystal oscillator; circuitry to provide power-on/restart and DMA functions; and 3-state, TTL-level buffers on the data and address lines. The second module, the debug, contains ROMs and RAMs, circuitry that provides an asynchronous serial data link between the EXORciser and a data terminal, plus bus and control interface logic.

EXbug™ software, a group of diagnostic/debugging and housekeeping routines, is masked in ROM. A MAID™ (Motorola Active Interface Debug) routine in the EXbug firmware permits examination and manipulation of the designer's program after it has been loaded into the EXORciser's memory. Two 128 x 8-bit RAMs store interrupt addresses and variable parameters.

The third basic module, the baud rate, is located in the back of the chassis. It completes an ASCII-formatted, duplex serial data path between the EXORciser and a data terminal. An asynchronous communications interface adapter plus 20-mA and RS-232-C level interface circuitry on the debug module, together with a bit rate generator on the baud rate module, allow connection of the EXORciser to a variety of terminals. Eight rates between 110 and 9600 baud may be chosen by a switch on the back of the chassis.



Motorola Semiconductor Products' EXORciser™ can be used for real-time emulation of M6800-based designs. Combinations of basic logic modules and optional memory, I/O, and special-function cards provide wide range for user in developing dedicated system

Additional options include a 2K static RAM module which permits assignment of two 1024 x 8-bit memory arrays to various address locations within 61 kilobytes of address space that is utilized for the prototype system design. (An additional 4 kilobytes of the address range hold the EXbug program.) An I/O module is available to link MPU and peripheral equipment. Peripheral interface adapters may be assigned to locations within the 61-kilobyte address space. Other currently available options are the universal wirewrap module, with 75 sockets for prototyping, and the extender module, which permits plug-in cards in the chassis to be raised above the top of the frame for access to the components.

A resident assembler/editor program, formatted in a variety of storage media, is offered as several packaged options. A source language for the M6800 system, built around the MPU's 72 mnemonic instructions and a set of 12 assembler directives, is used to create source programs. Assembler routines translate these source programs into MPU-understandable language (object codes), and editor routines are used by the designer for construction and modification of the programs.

An EXbug "load" routine transfers the resident assembler/editor software to the EXORciser memory. Debugging of and interaction with subsequent source programs is accomplished via other EXbug routines. Resident software is currently available in 12 options: a cassette, a floppy disc, a paper tape, services of the GE International Timeshare Network, or eight other formats containing 8 kilobytes of RAM plus one form of the storage media. Two memory configurations are offered: a module containing four 2K static RAMs and a module containing one 8K dynamic RAM module.

Circle 174 on Inquiry Card

μComputer Development System Is Hexadecimal Based

Up to 64 kilobytes of directly addressable RAM, p/ROM, or a combination may be ordered with the MicroPac 80/A microcomputer development system. Basic configuration of the hexadecimal-based system includes 8 kilobytes of RAM and 2 kilobytes of p/ROM, terminal interface, and control panel. A p/ROM programming system is also available.

Made by PCS, Inc, 5467 Hill 23 Dr, Flint, MI 48507, the system is compatible with a broad line of peripherals as well as I/O interface and communications modules. A basic operating system (BOS 80/A) residing in p/ROM, contains built-in power-fail-restart linkages and interrupt-debug capabilities. Other software features include a standalone macro-assembler.

A desktop (or alternate rack-mounting) enclosure contains room for the CPU and any combination of up to 15 memory or I/O modules. As many as 15 enclosures (up to 255 modules) can be attached through a "flexibus." The user can alter the module mix during development without rewiring the bus.

Circle 175 on Inquiry Card

Straight talk about IC sockets.

Integrated-circuit sockets are becoming such a household item, people are starting to forget something.

They're not all alike. And the differences can have a major impact on the performance and profitability of the products they're used in.

That's why we've decided to go over a few socket basics.

THE REASONS... AND THE RISKS.

All sockets serve basically the same purpose: they allow you to replace ICs without damaging either the IC or the PC board. In so doing, they make both design changes and field service economically feasible for you and your customer.

There's only one problem. When a socket fails, troubleshooting can be a nightmare—to a point where you'd have been better off without sockets in the first place. So it pays to be sure that the sockets you buy are right for your application.

CHOOSING THE RIGHT SOCKET.

Buying the right socket is much more than a matter of profile and price. It's matching the right one to the demands of your application.

For low-cost, high-volume products where the risk and consequences of socket failure are minimal—and where repeated IC insertion and high retention aren't required—buy the cheapest sockets that will do the job properly.

But for high-shock and vibration environments, or other situations where performance is critical, by all means get the best sockets money can buy.

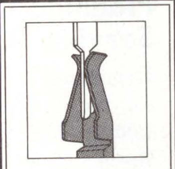
At Augat, we understand these differences. That's why we make sockets for both needs, in the widest range of sizes and specifications in the industry—from 6 to 40 contacts, on .300", .400", and .600" centers. These include low-profile, LED, and test sockets, socket carrier assemblies, and more—with PC, wire-wrapping, and solder pocket terminations.

And thanks to high-volume, automated production economies, these sockets are priced competitively despite many features you can't get elsewhere.

SMALL POINTS MAKE A BIG DIFFERENCE.

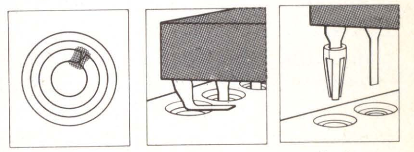
It's amazing how the finer points of socket construction can affect reliability.

Take the material the contacts are made of. For repeated IC insertion and good retention no other material can match the beryllium copper used in all Augat PC sockets. Cost alone leads other producers to use other materials.


The Augat method since 1965.

Designs vary, too. Among low-priced sockets, Augat's new low-profile series grip the IC lead along *both* flat sides, rather than by the edge, for best contact. And they'll take the full range of lead sizes, too.

Among premium sockets, Augat's Series 500 and 700 are the only ones in the world to include the two-piece machined contact assembly designed and perfected by Augat. While stamped "equivalents" abound, their looser tolerances have given rise to a series of pitfalls avoided by the Augat design:


The corroded contact. The bent IC lead. The loose contact.

In the important matter of flow soldering, both series again provide a decisive edge. The closed-end construction completely eliminates the possibility of flux or solder wicking.

These distinctions may seem small. But taken together, they're a good indication of how well the sockets you buy will stand up under long-term use. And in a market flooded with lookalikes, they're something to shop for.

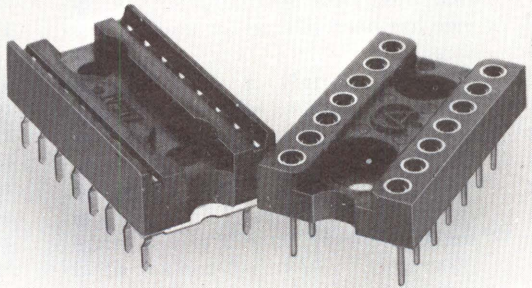
A SUPPLIER YOU CAN COUNT ON.

As the pioneer and leader in the IC interconnection industry, Augat has always been the world's prime supplier of IC sockets.

Now, after completing a multi-million dollar program of vertical integration, we're better equipped than ever to maintain that position—by providing the best sockets, the best service, and the finest distributor network in the world.

For all the facts, send today for our new brochure. We're convinced that the more you know, the more you'll come to Augat for all your IC interconnection needs.

YOU ONLY GET IT ALL FROM AUGAT.



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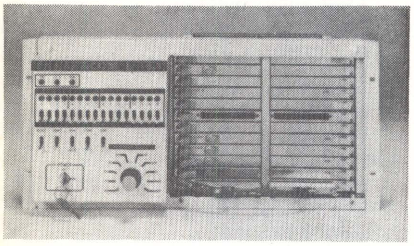
CIRCLE 56 ON INQUIRY CARD

G-P Microcomputer Has Capabilities of Minicomputer

Designed around three n-MOS/LSI circuits, the general-purpose PFL-16A microcomputer is said to provide an array of functions equivalent to minicomputer systems. Panafacom Ltd, PO Box 4637, Mountain View, CA 94040 claims that the system's architecture stresses ease-of-operation, modularity, and reliability and establishes cost/performance throughput that is "unparalleled in current 16-bit competitive offerings." Hardware architecture can support a varied complement of software modules for business, manufacturing, measurement, and control and communications.



The CPU circuit performs 16-bit parallel operations in 3 μs. Subchannel adapter (SCA) and the direct memory access channel controller (DMAC) circuits provide an I/O transfer rate capability up to 1 megabit/s. Hierarchical design supports an expanded set of standard cards that provide total hardware/software systems modularity and flexibility. Minicomputer features include five 16-bit registers; six addressing modes; three external level interrupts, priority multiple level interrupt; diversified arithmetic instructions; DMA; and extended memory capabilities.

To complement hardware concepts in the CPU circuit, I/O control is predicated upon achieving maximum systems throughput while supporting a broad assembly of peripheral devices. Throughput and support are achieved via the operations performed by the DMAC and SCA channels and subchannel arrangement. Based upon the systems requirements established by the end-user, the I/O design provides comprehensive flexibility through features such as DMA capability, byte or word data channels, attachment of 32 subchannels to CPU, asynchronous interface, selectable transfer modes, party-selectable data feature, program-specified subchannel modes, interrupt control functions, and readily attachable peripheral devices.

Software support modules also provide characteristics comparable to minicomputer offerings. Self-standing system (SSS) software contains program modules used for debugging hardware and software with links to the object program. Basic SSS support programs include initial program loader, micromonitor, I/O control subroutines, and arithmetic subroutines, as well as utility programs encompassing linkage loader, debugging utility, and ROM support utility. Support software under development includes cross-assembler and simulator programs written in FORTRAN IV. These programs will run on U. S. Timeshare and standalone computer systems.

Circle 176 on Inquiry Card

Microprocessor Product-Planning Consulting Service Available

Organized to be a continuing service for both users and manufacturers of microprocessors, a series of detailed studies, quarterly updates, data bank access, and other support are being introduced by Darling & Alsobrook, 1801 Avenue of the Stars, Los Angeles, CA 90067. The management consulting firm states that the service will act as "an essential product planning tool for both management and design personnel" and believes that this is the first time such a service has been offered for microprocessors.

The first study or volume in the series, available Dec 1, will cover the impact of the microprocessor on the analytical instruments industry. Advance subscribers will also receive two pre-release reports, "Microprocessor Technology" and "Current Microprocessors," which will contain significant late data and evaluations concerning microprocessors. Four quarterly update reports will maintain the timeliness of the basic volume, and will report on late introductions of microprocessors, software, and systems, as well as on developing trends in the use of microprocessors in analytical instruments. Following delivery of the final material for the study, a debriefing will be provided at each client's facility. At this time a principal of the consulting firm will further probe topics relating to the study and assure proper use of the information within the client's organization. Continuing update reports in 1977 and beyond will be made available separately.

The data bank service will enable clients to obtain detailed information through Dec 1, 1976, on microprocessors for analytical instruments. In addition, a range of proprietary services will be offered to purchasers of the study, including such areas as the evaluation of specific applications, corporate strategy consideration, and analyses of selected markets.

Chapter 1 of the analytical instruments volume will include general information on microprocessor history as an introduction to the remainder of the study. Chapter 2 will contain a comprehensive overview of microprocessor technology: chip design, architecture, memory devices and systems (RAMs, ROMs, and mass memories), I/O devices, software support and development aids, and application decisions (microprocessor vs minicomputer and microprocessor vs hardwired systems).

Chapter 3 will analyze the microprocessors currently available from each manufacturer, and Chapter 4 will provide extensive details on applications of the microprocessor to analytical instruments: control; instrument testing, calibration, and standardization; direct readout and data display; data logging, retrieval, and transmission; and application design, including microprocessor selection. Design examples for applications will also be discussed.

Chapters 5 and 6 will provide current market data as well as projections to 1982 for analytical instruments by type and use, and for each microprocessor application in this area. Breakdowns will be by microprocessor type, by instrument type, and for captive vs noncaptive.

Price for the Analytical Instruments volume of the Microprocessor Impact Series, four quarterly updates, pre-release reports, and other services is $6500. A prospectus describing the on-going program and the Analytical Instruments volume is available. Later volumes will cover studies on microprocessors in other application areas.

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Circle reader card 57 for PDP-8, 58 for PDP-11, 59 for Nova, 60 for Varian, 61 for H.P., and 62 for Interdata.

μProcessor Seminars

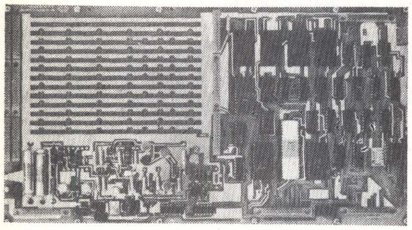
A series of seminars, conducted by Microcomputer Technique and sponsored by Cramer Electronics, has been scheduled for the last quarter of 1975. Each lasts three days and emphasizes "how-to" engineering aspects involving microprocessors.

Seminars will be held in 11 major cities in 1975, and plans are underway for an international program in 1976. Information about registration and the course outline details can be obtained from Microcomputer Technique, Inc. 11227 Handlebar Rd, Reston, VA 22091. Seminar fee is $395; attendance is strictly limited. Registered attendees are invited to view introductory video tapes at any of Cramer's offices to prepare for the course.

Circle 177 on Inquiry Card

Wirewrap Section On Microcomputer Board Simplifies Development

The MSC8080, an 8-bit single-board microcomputer from Monolithic Systems Corp, 14 Inverness Dr E, Englewood, CO 80110, includes a general-purpose wirewrap section to simplify computer/system interfacing. Intel 8080 microprocessor and interfaces for input, output, optional memory, and control panel as well as room for 1K x 8 of p/ROM are provided on the 7½ x 13½" board. A number of preprogrammed p/ROMs are available as options.



Connections from the processor board to memory, control panel, and I/O device are made by flat cable. A power inverter on the board supplies all necessary processor voltage levels from a single 5-V input. The microcomputer is completely compatible with the Monostore family of semiconductor memory systems.

Options are available to tailor it for use in specific system or for dedicated microcomputer development, including several semiconductor memory systems such as CMOS nonvolatile, low-power static, and high-density 4K RAM systems; control panel with pushbutton input, 4-digit hexadecimal LED readout, and teleprinter interface connection; and p/ROM software for memory test, processor checkout, TTY monitor and test, and edit. All I/O levels are TTL compatible.

Circle 178 on Inquiry Card

Study Predicts 60-Fold Increase in European Microcomputer Market

Total cumulative shipments of microcomputers in Europe over the 1974-84 decade are predicted to total $2.5 billion. A study by Frost & Sullivan, Inc, 106 Fulton St, New York, NY 10038, says that of this total, microprocessor components will account for $1 billion; memories $850 million, divided into read-only at 29%, read/write at 71%; I/O interfaces $550 million; and other ancillary circuits $75 million. 1974's $10 million level will expand to $600 million in 1984.

Industrial control, the "largest potential market" in Europe, will cumulatively total $720 million through 1984. Predominating will be production control applications in which microprocessors will replace existing hardwired controllers. Utilities will account for about 15% of the microprocessor market.

Laboratory equipment will account for $183 million worth of microprocessors, primarily for "smart" instruments; and data collection, entry, and communications markets will use nearly $1 billion worth of microprocessors, excluding that portion accounted for by IBM. Other markets will be transportation, building, environmental control, and word processing, accounting for $20 million worth of microcomputers in 1979 and rising to $200 million by 1984 for a cumulative consumption of $350 million.

"Europe" for this study consists of the eight European Economic Community countries—Belgium, Denmark, France, West Germany, Ireland, Italy, The Netherlands, and the United Kingdom. France, Germany, and the United Kingdom will account for over two-thirds of European microcomputer usage. Significant markets will also be present in Scandinavia, accounting for 6½% of total consumption; the Benelux countries, 8½%; and Italy, 5%.

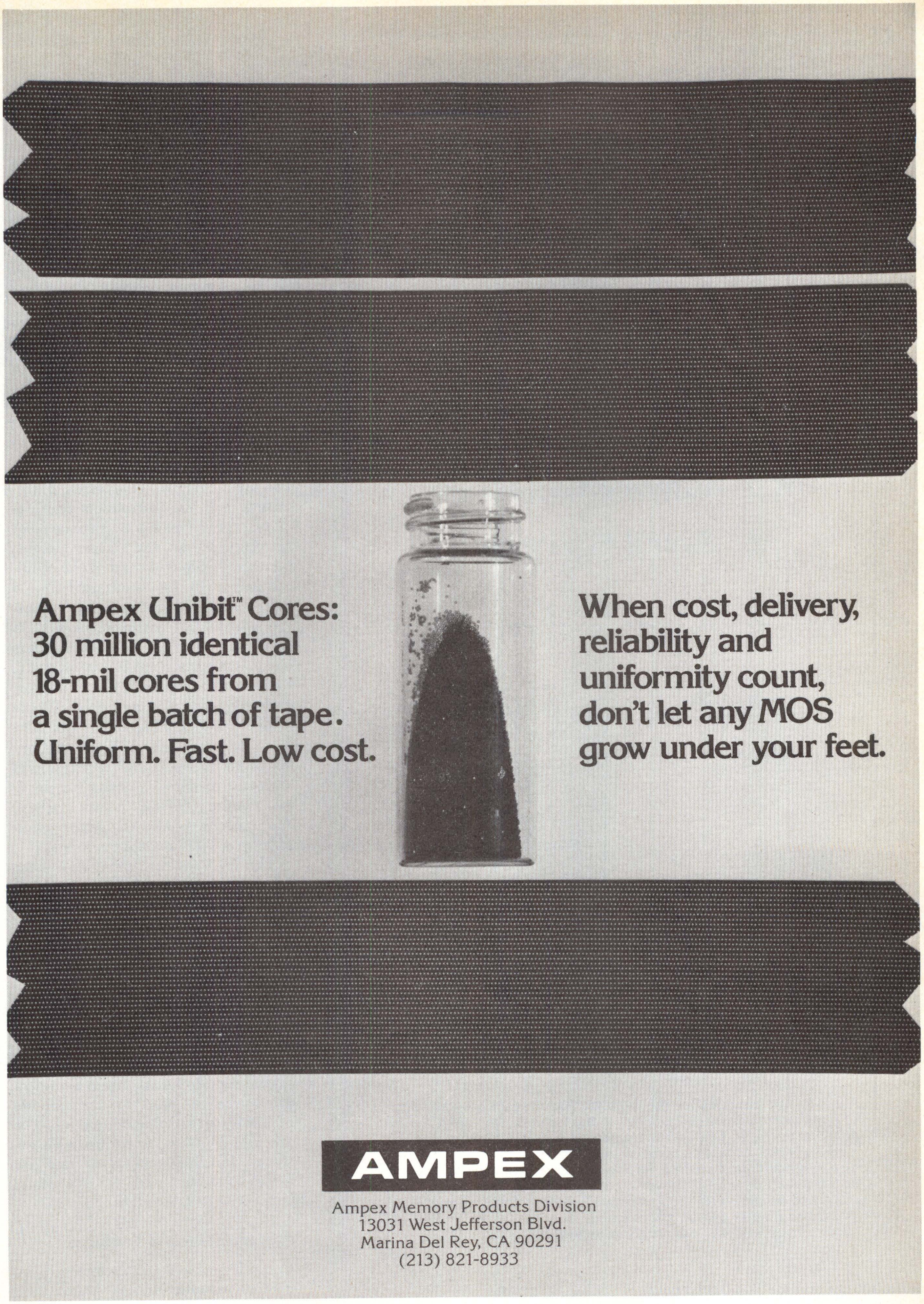
Circle 179 on Inquiry Card

Microprocessor Users Offered Advanced Software Capabilities

Designed to provide increased design flexibility and advanced software engineering capabilities to users of Intel 8008, Intel 8080, and DEC MPS series microprocessors, the Microprocessor Cross Assembler permits software to be designed and developed in-house under a real-time disc operating system. Offered by Innovonics Corp, 14119 Castle Blvd 402, Silver Springs, MD 20904, the cross assembler will also permit programs developed for the 8008 or the MPS to be directly translated into 8080 code with no user software modifications.

Significant features include more than 20 levels of error reporting to facilitate program debugging; symbolic addressing; FORTRAN type DATA initialization directive; extensive expression-evaluation capability; define word, define byte, text, and listing format-control directives; assembler directive and instruction mnemonic redefinition during the assembly process; symbol value redefinition during the assembly process; variable length symbol table allowing expanded symbol tables for larger host machine core memory installations; and absolute-load paper tape generation from predefined binary files. Output listing controls are provided for either 132-col line printers or 80-col terminals with a user selectable option of hexadecimal or octal output listings. □

Circle 180 on Inquiry Card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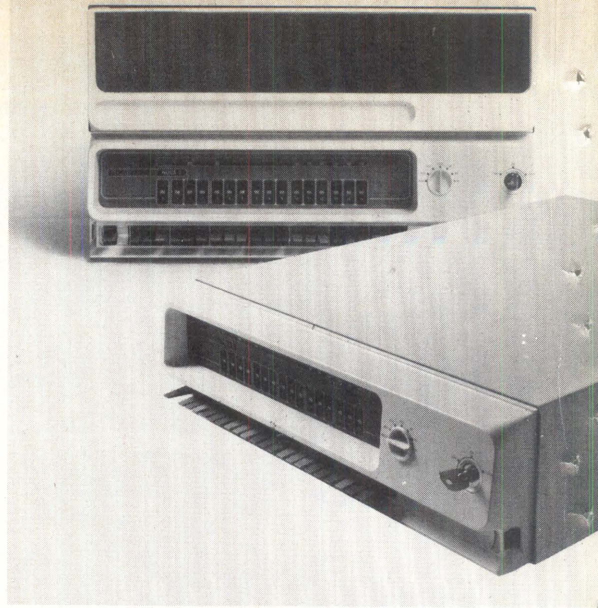
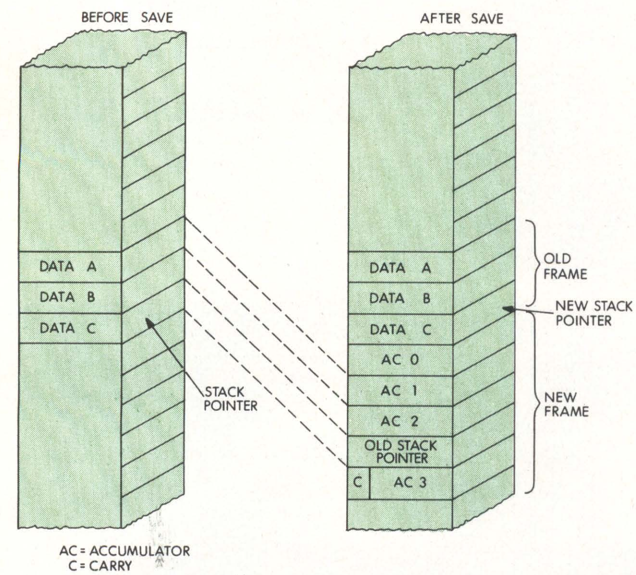


Minicomputer Family Combines Unique Architecture and Memory Capacity for Small Systems



A last-in, first-out (LIFO or "push-down") stack eases programming of real-time re-entrant subroutines in the Nova 3. Stack and frame pointers reside in CPU hardware registers and reference a main memory stack area. In operation, subroutine parameters and return information are pushed onto the stack by single-word "push" and multi-word "save" (shown here) instructions, and can be removed by single-word "pop" or multi-word "return" instructions. The frame pointer can be set randomly to access words stored in stack frames without "popping" an entire frame

Use of hardware data stack architecture and an instruction trap facility, plus memory management architecture in the larger model, permits Nova 3/4 and 3/12 minicomputers to be configured for a wide range of system capabilities. Choice of high performance n-MOS semiconductor or nonvolatile core memory (up to a maximum of 128K words for the model 3/12) is offered. Memory types may be mixed. Where n-MOS speed is desired but volatility is a problem, an optional battery backup with automatic recharge will maintain memory contents for up to two hours during power failure. Word parity is also optionally available for n-MOS memory systems.

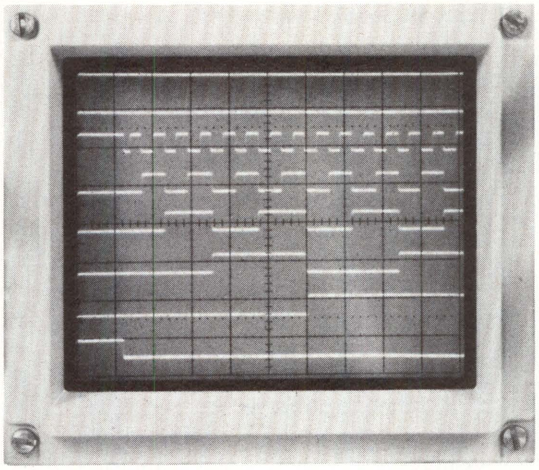
The medium to high performance family of 16-bit word length minicomputer systems is instruction- and peripheral-compatible with Data General Corp's other Nova minicomputers. All Nova line options and peripherals can be used. Systems are completely supported by software such as RDOS, FORTRAN IV, FORTRAN 5, ALGOL, and Extended BASIC.

Configurations fit a wide range of system requirements from a low of 4K words of MOS to a maximum of 128K of MOS and/or core. The 4K n-MOS chips were specially designed for this application and are being manufactured at the company's Sunnyvale facility.

Performance and Features

Comprehensive stack architecture includes variable frame length and

If your bench scope says your ECL logic looks like this...



...you're using the new 100MHz 8100-D Digital Logic Recorder from Biomation.

Introducing the new 100MHz Glitch Fixer: Biomation's 8100-D puts a faster fix on faster glitches.

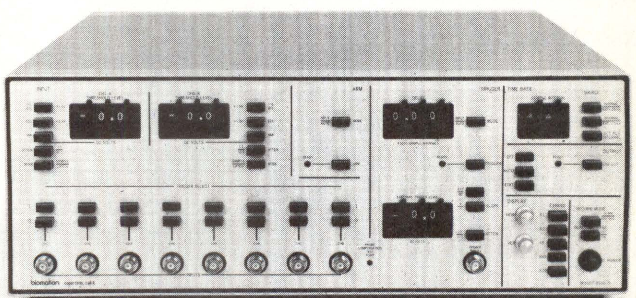
The original Glitch Fixer, Biomation's 810-D, has been helping a lot of engineers study timing relationships of 8-bit signals at speeds up to 10MHz.

But because the world's going faster—with MECL, ECL II, ECL III and Schottky-clamped I^2L parts in your boards—we've built a new digital logic recorder, the 8100-D, with speeds up to *100MHz*.

It's the new-and-faster way to turn your ordinary bench scope into a data stream display. It records 8 data channels at once and presents them in the same format you're used to seeing on data sheets.

The 8100-D features built-in combinatory logic setting to help you isolate your problem event *fast*. It has a big memory, too; can store up to 2,048 8-bit data words, including the often critical information that lies *just ahead* of the triggering event. And it also provides digital output for computer analysis or mass storage.

The 8100-D is a piece of diagnostic instrumentation that circuit designers and troubleshooters have been asking us for. We will be glad to send you all the splendid details. Just use the reader service number or get in touch with us directly. Biomation, 10411 Bubb Road, Cupertino, CA 95014. (408) 255-9500. TWX 910 338 0226.



biomation

CIRCLE 64 ON INQUIRY CARD

powerful state-save instruction capabilities implemented with CPU stack and frame pointer registers. The stack facility contains one stack pointer and one frame pointer. State-save and restore commands are at 5.2 and 4.8 μs, respectively; register "push" and "pop" stack commands are 1.4 to 1.5 and 1.7 μs, respectively.

Memory management hardware offers dual program-space maps and expanded data channel map capability. Dual mapped program space is allocatable in 1K-word increments via 32 registers in both program spaces. Each of 64 data channel map registers addresses a 1K-word space. Physical (unmapped) program space is 32K words.

Multi-accumulator architecture is 16 bits, with an efficient single-word, multi-function instruction set. 1K words can be directly addressed via absolute, relative, and indexed modes; 32K words can be indirectly addressed on a multi-level basis (128K with memory management). Memory-based stack addressing is on both a last-in, first-out basis and random using indexed addressing.

Included in each unit are four accumulators and 18 index registers—two hardware, 16 memory. Both a standard high speed direct memory access (DMA) data channel and a 16-level priority interrupt structure are operable in CPU "run" or "halt" states. Maximum DMA word transfer rate is 1.1 MHz.

Units have separate memory and input/output buses. I/O bus levels are ground and 3 V. The I/O system is 16-bit word length and has 16 priority interrupt levels. 61 devices are addressable.

Each minicomputer chassis is configured with slots for various boards: four in the 3/4 and 12 in the 3/12. A 12-slot expansion chassis can be added to the 3/12 for large systems. Slots in the 3/4 hold a CPU, power fail/auto restart, auto program load board; a memory board; choice of a second memory board or an option board with multiply/divide and/or parity logic for the optional parity on MOS; and a peripheral interface board. The 3/12 contains CPU board; an option board containing any combination of memory management, multiply/divide, and parity control; as many as eight memory boards; and up to three peripheral interface boards; the expansion chassis can hold 12 peripheral interface boards. System memory and I/O buses are carried in the CPU mainframe but only the I/O bus is available in the expansion chassis.

MOS memory boards are available in 4K-, 8K-, and 16K-word increments; memory cycle time is 700 ns. Core memory is available in 8K-word boards with 800-ns cycle time and 16K-word boards with 1-ms cycle time. Full 128K-word capacity is attained in the 3/12 by using eight 16K-word boards.

Since the n-MOS memory chip was designed specifically for use in the company's computers, rather than for sale separately, it was possible to obtain benefits that might not otherwise have been attained. Output is non-TTL; a bipolar sense amplifier boosts the chip's natural output to the TTL level. In addition, a TTL clock driver was designed which also provides significantly higher performance. The decision to design a 20-pin chip gives space advantage on the board without a sacrifice in speed. All need for multiplexing has been eliminated by the design features.

General Specifications

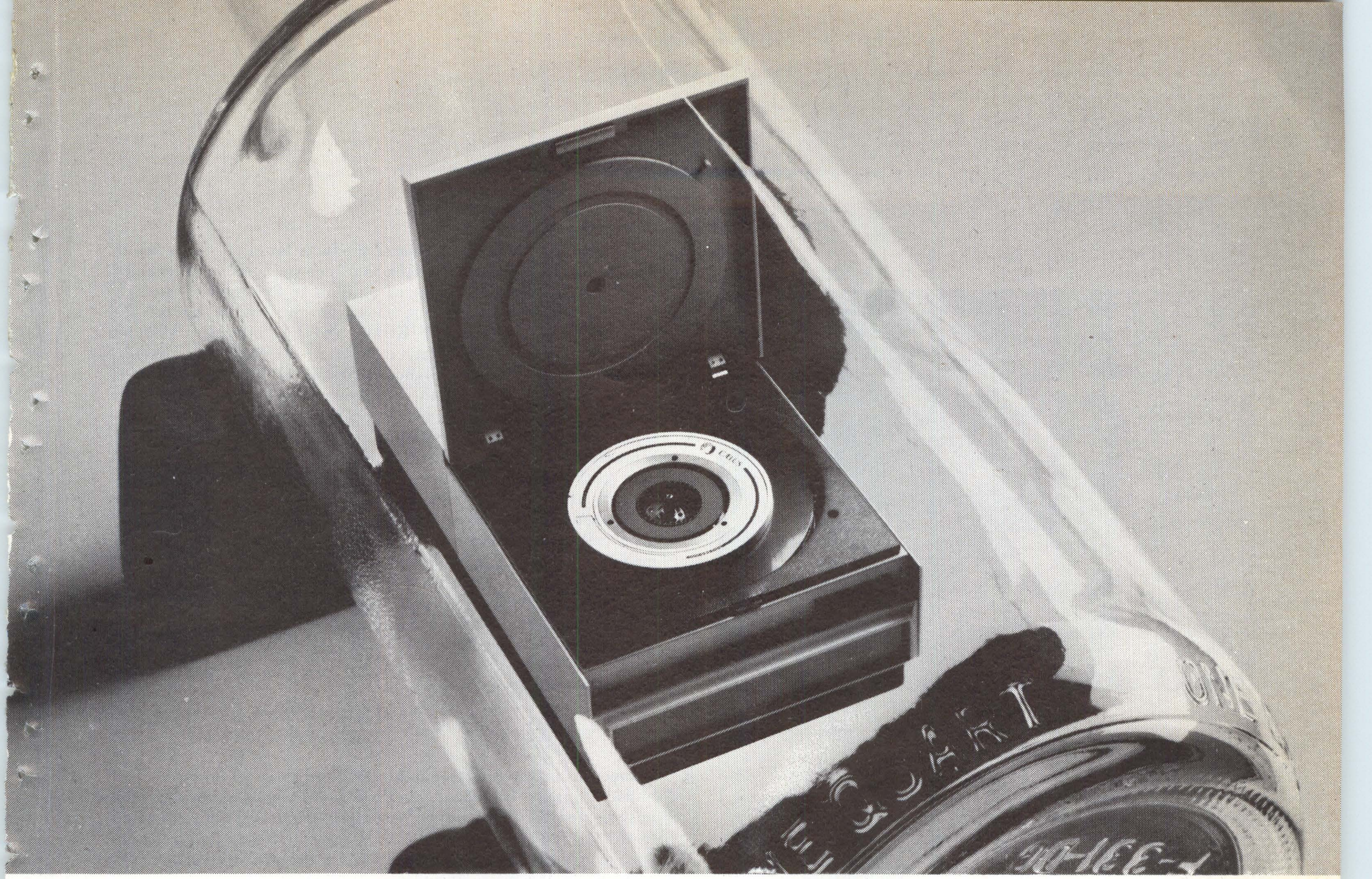
Power requirements are 115 V ±20%, 10 A, or 230 V ±20%, 5 A; 47 to 63 Hz, single phase; with 900-W max power dissipation. Unit dimensions are 5¼ x 19 x 23" for the 3/4 and 10½ x 19 x 23" for the 3/12. Weights are 40 and 100 lb, respectively, fully loaded. Heat generated is 1000 and 3000 BTU/hr max.

Temperature ranges are 0 to 55°C at 90% RH operating, −35 to 70°C at 95% RH storage. Altitude ranges are to 10,000 ft operating, 50,000 ft storage.

Price and Delivery

Because of the advanced status of information received from the manufacturer, prices for the Nova 3 family were not available at press time. However, the 3/4 and 3/12 and memory boards will be sold on an OEM basis with applicable quantity discounts. Delivery times are 30 days ARO for the 3/4 and 60 days ARO for the 3/12. Data General Corp, Southboro, MA 01772. Tel: (617) 485-9100.

For additional information circle 199 on inquiry card.



Big technology for Mini-computers.

The mini-computer market has grown to the point where it demands "3330" disk technology in a package that fits.

Introducing:
The Trident Disk Drives.

Greater track density helped get us down to size. The new Trident Series brings you 370 tracks-per-inch. And up to 6,060 bits-per-inch. Storage capacities range from 27-82 megabytes.

Designed for the OEM.

The Tridents are each compact, self-contained and rack-mountable.

Their start or stop time is only 20 seconds. Pack changes take less than one minute. Rotational speed is 3600 r.p.m. Track access time is 6 milliseconds.

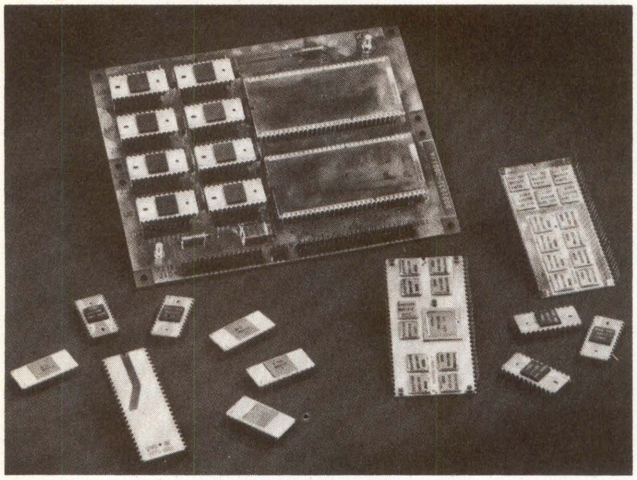
The Trident Series has one of the lowest cost-per-byte ratios in the industry.

These features make the Tridents easy to buy and easier to sell. Call or write California Computer Products, Inc., CD-10-75, 2411 West La Palma Avenue, Anaheim, California 92801. (714) 821-2011.

CALCOMP

PRODUCTS

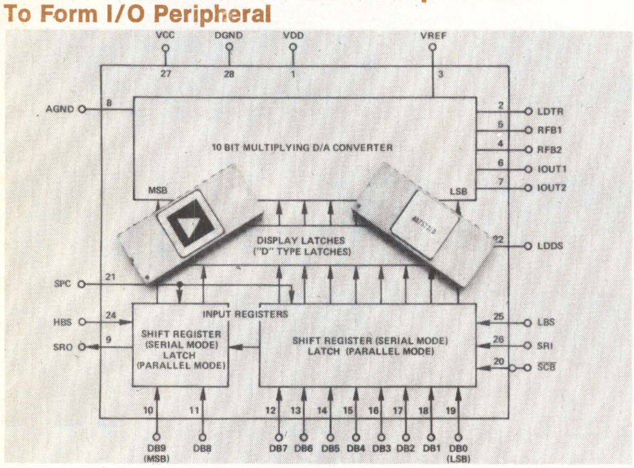
Unbundled Microcomputer Offers Designer Choice of Control Components and Modules



Flexibility in the design of control products for applications where standard microcomputer systems may not be suitable is enabled by a plan that permits choice of portions to fit a specific requirement. Series 300 components, shown in the bottom left of the photo, include interpreter, p/ROMs, and I/O interface. Modules or subsystems, bottom right, include processor, I/O interface, and read/write storage. (Standard System 20 MicroController is in background.) The 48-pin interpreter is a monolithic, bipolar Schottky microprocessor capable of executing complete instructions within 300 ns. It contains an 8-bit ALU and eight 8-bit scratchpad registers. Communication is via instruction and I/O data paths. All I/O pins are TTL compatible. Interface components are 8-bit I/O registers, one with 3-state outputs and one with open-collector input, in 24-pin packages. A wide range of standard memory and support circuits can be used. Processor module includes interpreter and 512, 1024, or 2048 16-bit words of ROM program storage. R/W storage module contains 256 bytes of bit-addressable bipolar memory. A starter kit provides interpreter, four I/O interface packages, and six 512 x 8-bit p/ROMs. **Scientific Micro Systems,** 520 Clyde Ave, Mountain View, CA 94043.

Circle 200 on Inquiry Card

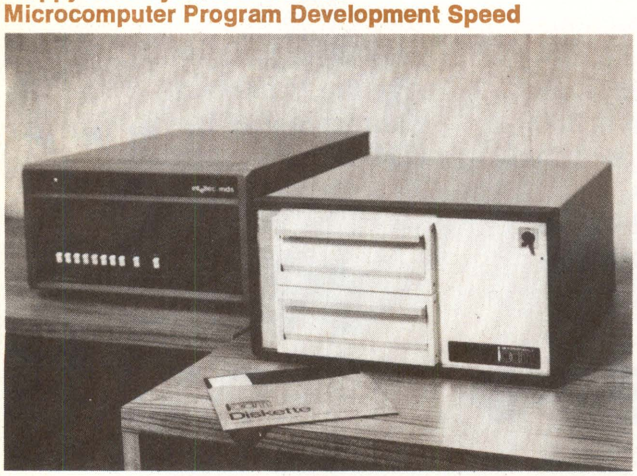
D-A Converter Interfaces With Microprocessors To Form I/O Peripheral



Claimed to be the first monolithic D-A converter featuring double-buffered inputs for direct interfacing with microprocessors, the bus-oriented AD7522 can be selectively addressed and therefore treated as an output peripheral. Double-buffered digital inputs enable provision of an analog output for the previous digital message, while the microprocessor is loading a new value into the DAC's front buffer (which can also be loaded in a serial fashion). CMOS construction limits quiescent I_{DD} supply current to 2 mA max. Resolution is 10 bits with linearities, depending on model, of 8 bits ±0.2%, 9 bits ±0.1%, or 10 bits ±0.05%. Differential nonlinearity tempco is ±2 ppm/°C max; gain tempco is ±10 ppm/°C max. With a 5-Vdc logic supply, it interfaces with TTL; with 15 Vdc, it interfaces directly with CMOS. A 15-Vdc power supply is also required. The DAC, counterpart to the 10-bit CMOS AD7570 ADC, is available with 0 to 75°C temp range in 28-pin plastic or ceramic DIPs, and −55 to 125°C in ceramic. **Analog Devices, Inc,** PO Box 280, Rt 1 Industrial Pk, Norwood, MA 02062.

Circle 201 on Inquiry Card

Floppy Disc System Increases Microcomputer Program Development Speed

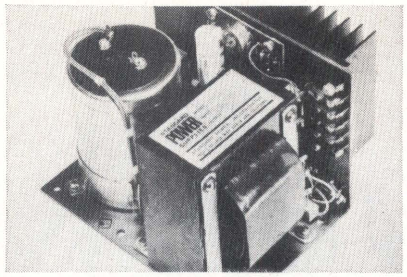


Fully hardware and software compatible with Intel's Intellec MDS-800, the FD360-53 floppy disc system speeds up program development for MDS users. Interconnection is through a ribbon cable to an interface card that plugs directly into the MDS chassis; installation requires <5 min. The interface card contains a 512-byte p/ROM which is preprogrammed with the floppy disc driver software. An operating system software package, supplied on a diskette, contains assembler and editor and features variable length files, automatic file packing, and automatic file creation. Possible single command operations are memory program loading, disc-to-disc editing, asssembling and file transfer, disc-to-paper tape transfer, and paper tape-to-disc transfer. Files can be created and maintained with either hexadecimal object or program source data. Special features of the controller/formatter, which provides full compatibility with IBM 3540 and 3740 formats, include separate read and write data buffers, hardware track seek and verification, and complete hardware CRC generation and verification. System storage capacities range from 256 kilobytes to more than 1 megabyte, using one to four disc drives. **iCOM Inc,** 6741 Variel Ave, Canoga Park, CA 91303.

Circle 202 on Inquiry Card

PRODUCTS

CONSTANT-CURRENT STD POWER SUPPLIES



Seven dc power supplies control current to within 0.1% and have compliance voltages from 8 to 30 Vdc, in adjustable current ratings from 0.1 to 15 A. All models operate on 115/230 Vac, 47- to 440-Hz inputs, and provide line/load regulation to 0.1% (min load to short circuit). Ripple is 0.1% typ, and response time is 50 μs. **Standard Power, Inc**, 1400 S Village Way, Santa Ana, CA 92705.
Circle 203 on Inquiry Card

5" CRT

This 5", 3½-lb CRT is offered as an enhancement to the company's portable Telecomputer™ and Data Line Monitor product lines. A specially designed briefcase to house either product plus the CRT makes each one extremely portable at approx 20 lb. **Digi-Log Systems, Inc**, Babylon Rd, Horsham, PA 19044.
Circle 204 on Inquiry Card

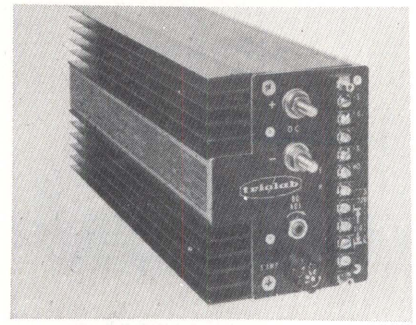
p/ROM PERSONALITY MODULES

Through use of five plug-in, interchangeable modules, the company's series 90 p/ROM programmer can now program Intel 2704 and 2708; MMI 6335, 6340, 6300/01, and 6305/06; and Intersil 5603/23, 5604/24, and 5600/10. Modules include zero insertion force p/ROM sockets for master and copy p/ROMs; binary data display for 4- or 8-bit copy p/ROMs; specialized interface circuits, regulators, and program instructions for specific p/ROMs; and control switches as required to implement special functions. **Pro-Log Corp**, 852 Airport Rd, Monterey, CA 93940.
Circle 205 on Inquiry Card

DELAY GENERATOR

Combining a crystal-controlled digital time base with an analog vernier, model 989 achieves delays to 50 s with fractional nanosecond resolution and resettability. Crystal oscillator gives simultaneous outputs in 9-decade steps plus division by 2 and 5—a total of 27 phase-locked frequency/time outputs. Selected digital outputs are then used to trigger analog delays, which interpolate between the crystal references. Four independent analog outputs are provided. **Instrument Research Co**, PO Box 231, Lincoln, MA 01773.
Circle 206 on Inquiry Card

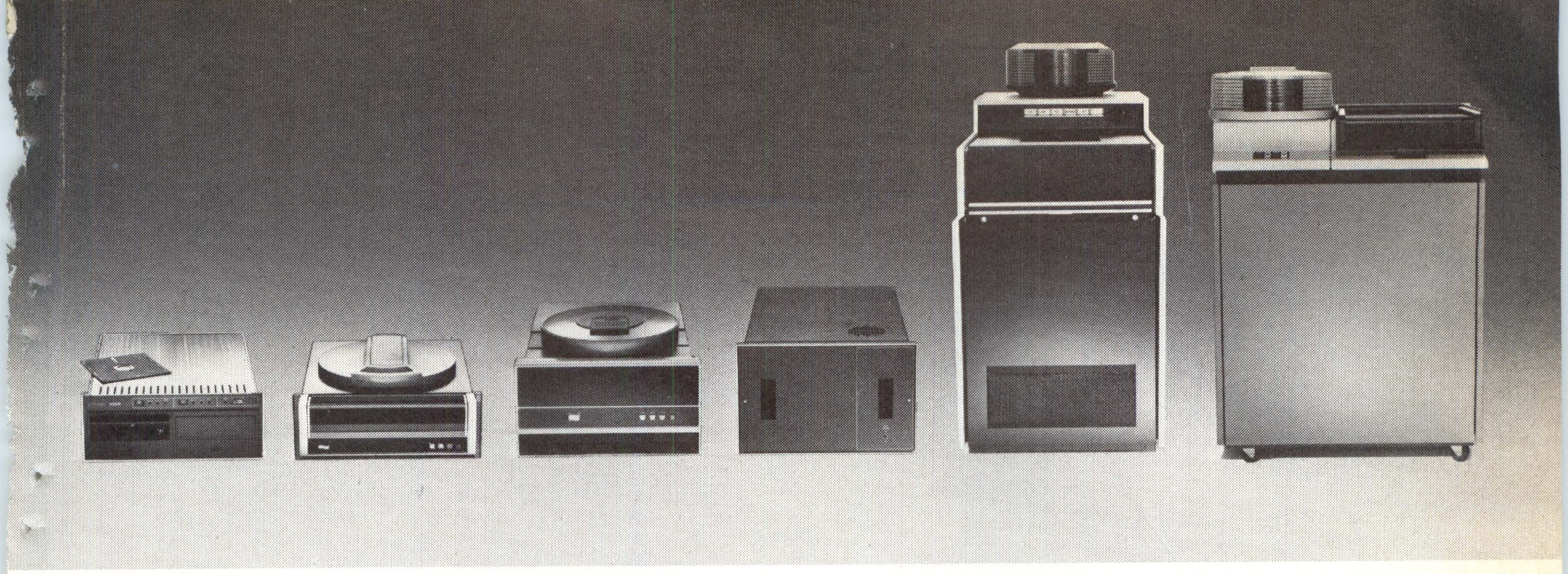
SWITCHING REGULATOR POWER SUPPLY



The 175-W series 672 delivers up to 35 A in a 202-in.^{3} package and will have UL recognition. Conversion efficiency is >70% with no audible noise. Fixed output voltages of 2 to 48 Vdc can be provided. Input is 102 to 130 or 198 to 256 Vac, 45 to 440 Hz, 1ϕ, selected by front-panel connection. Static regulation is ±0.2% output voltage change for worst line/load combination; dynamic regulation is 1% for each 10% of load current step with recovery to static regulation band in 300 μs. **Trio Laboratories, Inc**, 80 Dupont St, Plainview, NY 11803.
Circle 207 on Inquiry Card

PRECISION HIGH VOLTAGE POWER SUPPLIES

Series 205A lab devices feature linear circuit techniques resulting in accurate and stable high voltage output. Outputs range from 0 to 1 kVdc at 30 mA to 0 to 50 kVdc at 0.3 mA. Included as std are digital voltage controls, front-panel voltage and current metering, remote voltage and current monitoring, remote voltage and resistance programming, and reverse polarity. Regulation-ripple are 0.001% and tempco is 50 ppm/°C. **Bertan Associates, Inc**, 180 Miller Pl, Hicksville, NY 11801.
Circle 208 on Inquiry Card



Six of the best reasons for buying Data General computer systems.

If a computer system can't do a good job of file handling, chances are it won't do your job well either.

So we give you a lot of good ways to handle your files.

We offer six different disc subsystems. From 0.3 to 360 megabytes in size; with transfer rates from 30K to 800K bytes per second; and prices from $2,900 to $110,000. So you can pick out the ones that work the way you work.

And we fully support all our disc drives with our systems software. With RDOS and MRDOS for example, you can keep your high-use data on fast access discs, and data you need less on slower discs. With INFOS, you can logically partition a file across different physical media to get the most efficient use of your system peripherals.

All our operating systems treat all our peripherals like files. Which makes our files device independent. And a lot easier for you to use.

And because all our operating systems share the same file structure, you can maintain and operate your files with any of our languages: FORTRAN, BASIC, ALGOL, RPGII, MACRO assembler.

And you can use any combination of disc drives. So you can manage files from one to one billion bytes and match your file handling to your application.

Yet with all the flexibility we give you, we don't demand a lot in return. You can get an Eclipse S/200 system with 48K bytes of core and a 10 megabyte disc file for under $30,000. (quantity one, list price.)

Write for more information.

You may end up buying our computer systems because of the way we handle your files.

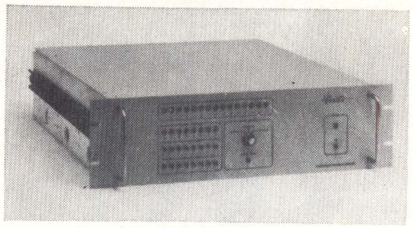
DataGeneral

Data General, Route 9, Southboro, Mass. 01772 (617) 485-9100. Data General (Canada) Ltd., Ontario,
Data General Europe, 15 Rue Le Sueur, Paris 75116, France. Data General Australia, Melbourne (03) 82-1361/Sydney (02) 908-1366.

CIRCLE 69 ON INQUIRY CARD

PRODUCTS

A-D CONVERTER

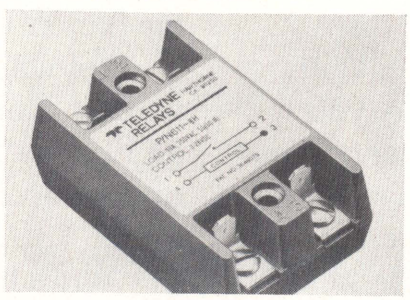


Model 2116, a 16-bit converter, features 2.5-μs conversion time, ±0.005% plus ½ LSB full-scale accuracy, 1-ns aperture time, 5-ppm/°C tempco, ±10-V full-scale input level, ±20-V max input, and >20-MΩ input impedance. Contained in a 5¼" high rack-mounting cabinet, it is available as a single-channel converter or with an input multiplexer, instrumentation amp per channel, and/or simultaneous S/H amps. **Tustin Electronics Co,** 1431 E St. Andrews Pl, Santa Ana, CA 92705.
Circle 209 on Inquiry Card

UNINTERRUPTIBLE POWER SYSTEM

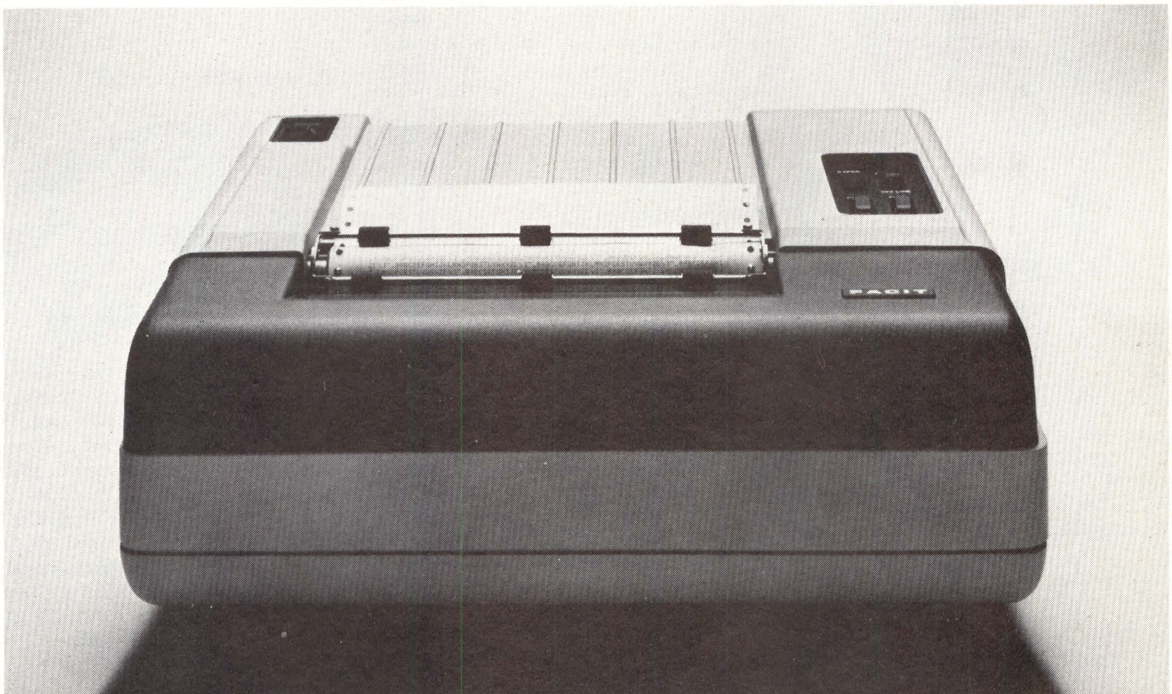
Designed to give the minicomputer user the protection normally justifiable only on larger systems, UPS can supply 115 or 230 Vac to a 1-kW load for either 15 or 30 min. Output is both voltage and frequency regulated to insure continuous "clean" power; furthermore, output is totally isolated from the power line. **Synergetic Scientific Systems, Information Products Div,** PO Box 926, Gainesville, FL 32602.
Circle 210 on Inquiry Card

SOLID-STATE RELAYS



Models added to the 611 series ac line include -7 (10 A/140 Vac), -8 (10 A/250 Vac), and -8H (10 A/250 Vac), which provides a 600-V peak transient immunity capability to prevent false triggering due to high line transients and inductive load switching. All feature logic-compatible 3- to 28-Vdc input, high dv/dt capability (typ 200V/μs min), and zero voltage turn-on/zero current turn-off. **Teledyne Relays,** 3155 W El Segundo Blvd, Hawthorne, CA 90250.
Circle 211 on Inquiry Card

Through a miracle of modern technology, Facit can now offer you less for your money.



Introducing the Facit 4554, with only two moving parts in the printing head.

The rationale: fewer parts moving around means fewer parts wearing out.

But we didn't stop there.

We also gave considerable thought as to how well our page printer should produce a print-out.

So, unlike most page printers, our 4554 uses a character by character (asynchronous) print-out and an automatic ribbon control to give you big, easy-to-read characters at 6 or 60 characters per second.

And whether you need one, two or even three copies, your print-out will always come out crystal clear.

Our 4554 is even less trouble to hook up than most page printers. That's because we give you several interface versions. Among them are: The Facit SPI interface for bit parallel data transfer, and the EIA, RS 232C.

All things considered, the Facit 4554 page printer is one of those rare instances where less for your money is really more for your money.

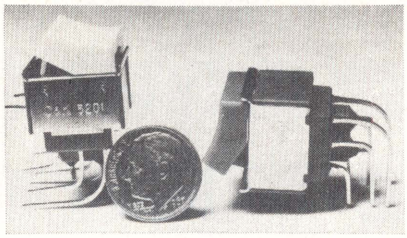
Facit-OEM Division,
66 Field Point Road,
Greenwich, Connecticut
06830.

FACIT
Dedicated to Efficiency

In Canada: Facit-OEM Division,
2270 Speers Road, Oakville, Ontario,
L6J-SK2 Canada.

PRODUCTS

ROCKER SWITCH WITH RIGHT-ANGLE TERMINALS



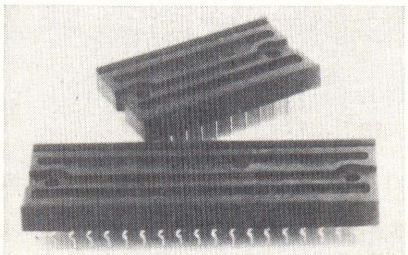
AV2 is an illuminated rocker with right-angle PC mounting terminal. Mounting angle is beneficial where std vertical mounting terminals will not fit or would demand costly internal instrument rewiring. Contact material is gold-plated brass, and switch is available in 1- or 2-pole models. **C&K Components, Inc,** 103 Morse St, Watertown, MA 02172.
Circle 212 on Inquiry Card

600-LINE/MIN. PRINTER

Printer is designed for use with the company's model 340 and 350 intelligent terminals and model 440 clustered-terminal processing system. Drum printing unit may be run by cassette, flexible disc, or magnetic tape drives, producing an original and up to five carbon copies on continuous, fan-folded, pin-fed forms measuring from 3.5 to 9.5" wide. **Sycor Inc,** 100 Phoenix Dr, Ann Arbor, MI 48104.
Circle 213 on Inquiry Card

LSI CONTACT SOCKETS

On 324-AG (24-contact) and 340-AG (40-contact) series, beryllium copper contacts meet on the flat surface of both sides of LSI leads. Sockets offer closed, tapered entry insulator design with large contact openings for quick LSI insertion and full seating. Termination styles include straight lead for smaller PC hole sizes, and "dap" lead which holds the socket in place on PC board during wave soldering. Low profile provides closer center-to-center spacing of parallel PC boards as well as positioning for maintaining continuous 0.1" spacing. **Augat Inc,** PO Box 779, 33 Perry Ave, Attleboro, MA 02703.

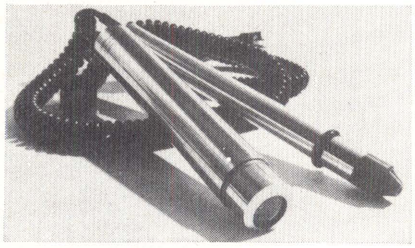


Circle 214 on Inquiry Card

PCB EDGE-LIGHTED PANELS

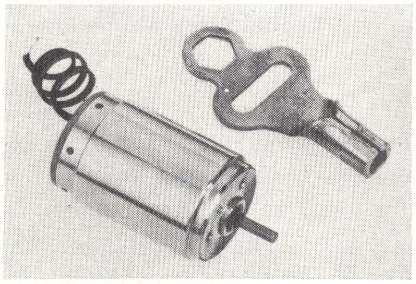
Aerospace optics technology is used in the design and manufacture of these high performance, repairable type V panels. Lamps are attached to replaceable circuit boards. Panels meet MIL-P-7788 and -8335. Uniform brightness is maintained at rated and low voltage. Mil and commercial colors are available. **Aerospace Optics, Inc,** 7112 Burns St, Fort Worth, TX 76118.
Circle 215 on Inquiry Card

LIGHT PEN SERIES



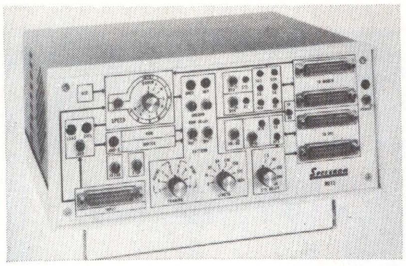
Two series, designed for symbol sensing, editing functions, and graphics, feature touch-actuated switching and no moving parts. LP-300 has a finder beam projected through its optical system to illuminate acceptance area of as small as 20-mil dia, and eliminate parallax problems. Response time is <300 ns. LP-200 features interchangeable tips. **Information Control Corp,** 9610 Bellanca Ave, Los Angeles, CA 90045.
Circle 216 on Inquiry Card

DC MICROMOTORS



With a frame dia of 28 mm, escap[R] 28 PL series, at rated voltages, have typ no-load speed of 5000 rpm and a range of stall torques to 8 oz-in. Torque constants are to 9.9 oz-in./A. Unloaded mechanical time constants range from 13 to 17 ms. Devices utilize an ironless rotor consisting of a cylindrical self-supporting skew-wound coil tolerating 100°C max. High stall torque, low moment of inertia, and small electrical time constant allow for several hundred start/stop cycles per second. **Portescap U.S.,** 730 5th Ave, New York, NY 10019.
Circle 217 on Inquiry Card

BUFFERED DATA TRANSMISSION SIMULATOR



BDTS is a programmable message generator for exercising data communications systems. System installation/repair time is reduced by testing modems, terminals, or controllers with actual polling sequences under simulated operating conditions. It may be used to debug hardware and software by testing new communications protocols online without need for CPU time. Data streams may be stored in 1024 bytes of customer-specified ROM and/or RAM. Transmission may be synchronous or asynchronous, 5 through 8 bits/char, and at any of 16 std communications rates. **Spectron Corp,** Church Rd & Roland Ave, Mount Laurel, NJ 08057.
Circle 218 on Inquiry Card

DISC CONTROLLER

Models 114, 213, 214, and 215 Calcomp disc memories can be added to any Varian series 620 or V70 minicomputers using type 70-5032 controller. It operates from PMA, DMA, or HDMA channels, includes its own cycle-steal hardware, and fits into the std Varian I/O slots. **Information Displays, Inc,** 150 Clearbrook Rd, Elmsford, NY 10523.
Circle 219 on Inquiry Card

TEMPERATURE-INDEPENDENT MEMORY CORES

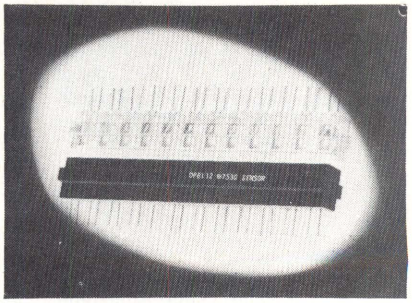
Two uniform-drive 18-mil cores compatible with industry-std medium-temp cores, UNITEMP cores operate with UNIform drive at TEMPeratures of −10 to 90°C. Cores withstand high disturb ratios and provide wide stack operating margins over the full 0 to 70°C range without drive current compensation. Types 2230 and 2244 operate with drive currents of 580 and 750 mA, respectively; all are 100% tested and inspected to 0.015 AQL. **Control Data Corp, OEM Computer Memory Products,** 3857 Louisiana Ave, St. Louis Park, MN 55426.
Circle 220 on Inquiry Card

TRIPLE-OUTPUT SWITCHING POWER SUPPLIES

Designed for OEM computer peripheral applications, supplies provide single voltage output for driving IC logic and dual voltage output for driving op amps and A-D converters. These 20-kHz inaudible switchers operate from a selectable input of 115/230 Vac, 47 to 63 Hz; output is 5 V at 50 A, ±12 V at 5 A, ±15 V at 4 A. Overvoltage protection is built into the single output, optional on the dual. Overload protection is std and EMI is minimized by shielding and filtering. **ACDC Electronics,** 401 Jones Rd, Oceanside, CA 92054.
Circle 221 on Inquiry Card

PRODUCTS

12-CHANNEL CARD READER ASSEMBLY



Two modules make up OPB 112: one containing an array of GaAs IR LEDs; the other, an array of npn silicon phototransistors. Assembly offers 12 channels spaced at 0.25" to match row spacing of std punched cards. Built-in collimating lenses on both modules eliminate crosstalk between channels; and noise from background illumination is eliminated by an optical filter. Also featured is a 0.02 x 0.04" aperture over each sensor. With assembly modules at a separation distance of 0.05", typ sensor output is 2 mA with LED input of 40 mA. **Optron, Inc,** 1201 Tappan Cir, Carrollton, TX 75006.
Circle 222 on Inquiry Card

120-CHAR/s SERIAL PRINTER

Series 1000 132-col, multi-copy desk unit features a needle printing method, microprocessor-oriented electronics, cartridge ribbon, and tractor engagement above and below the print line. Char-by-char visibility is achieved with a technique that moves the printhead a fixed number of columns after a pause in the printing operation. Model 1120 provides an original plus four copies on form widths from 4 to 15". Specs include 6 lines/in., 10 char/in., 64-char ASCII set, and 9 x 7 half-space matrix char. **Tally Corp,** 8301 S 180th St, Kent, WA 98031.
Circle 223 on Inquiry Card

SOLID-STATE RELAY

The S505-SJ series meets Class I VDE European requirements, or is available with direct CMOS (10 V, 1 mA) input, eliminating the need for power amplification. The relays range from 2.5 to 40 A and up to 810 PIV for European 380-V lines, and have zero voltage switching with an internal snubber network. The devices operate from 24 to 250 Vac, and provide 2500-Vac isolation. Input is 3 to 32 Vdc. Output specs include 120 Vac, 47 to 63 Hz, line voltage; 200 Vdc peak repetitive blocking voltage. **Electronic Relays, Inc,** 7106-08 W Touhy Ave, Niles, IL 60648.
Circle 224 on Inquiry Card

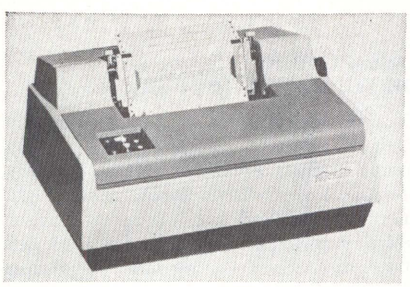
1024-BIT SCHOTTKY RAM

Static Schottky TTL 1024 x 1-bit RAMs, IM55S08 and -18 provide open-collector and 3-state ouputs, respectively, and contain on-chip address decoding and chip-select capability. Both are available in CERDIP packages in commercial (0 to 75°C) and military (−55 to 125°C) temp ranges. The -08 is equivalent to the N82S08, and and both are replacements for 93415/25 RAMs. Typ access time is 45 ns; input current is 250 μA max. Max read/write cycle times are 70 ns for commercial and 75 ns for military devices. **Intersil, Inc,** 10900 N Tantau Ave, Cupertino, CA 95014.
Circle 225 on Inquiry Card

1" LED DISPLAY

Single-digit "light-pipe" series 1720R/1723R feature 1" high char designed for ~60', single-plane, >160-deg viewing. Displaying 0 to 9 with right-hand decimal point, and available with either common anode or common cathode, units are slimline configured in an electrically nonconductive, plastic compound base with 14-pin DIP connections on 0.6" spacing. GaAsP material provides max brightness-to-current efficiency with pk light emission in the visible red spectrum at 655 nm. **Industrial Electronic Engineers, Inc,** 7720-40 Lemona Ave, Van Nuys, CA 91405.
Circle 226 on Inquiry Card

IMPACT PRINTER



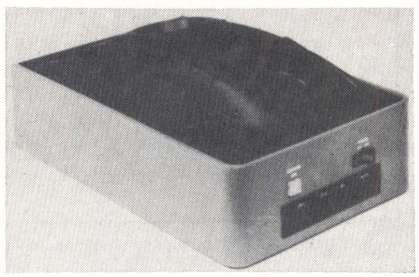
With plug-in compatibility to HP 9800 series programmable calculators, model 9306 can be utilized as the primary printer or as an addressable secondary printer in the system. Each self-contained unit includes electromechanical components and all electronic logic required for interfacing and char generation. It produces an original plus up to four carbon copies, with paper supply located below or to the rear. Std 64-char set can be expanded to 128; elongated boldface char may be printed on command. Print speed is 100 char/s using std 5 x 7 dot matrix. **Spantronics Engineering,** 702 Bowling Green, Moorestown, NJ 08057.
Circle 227 on Inquiry Card

PRODUCTS

CENTRIFUGAL BLOWER

A high volume, min space centrifugal blower that operates at a low noise level, the double-inlet unit delivers 1525 cfm with a min back pressure of 0.6" H_2O when operated at 115-Vac, 60-Hz, single-phase. Shut-off occurs at 1.45" H_2O. Measurements of 15½ x 15⁹⁄₁₆ x 10½" are achieved through use of a double-inlet centrifugal blower wheel that uses little space and permits the motor to be mounted inside the package envelope. Installation may be horizontal or vertical. **McLean Engineering Laboratories, Inc,** 70 Washington Rd, Princeton Junction, NJ 08550.
Circle 228 on Inquiry Card

ORIGINATE/ANSWER ACOUSTIC COUPLER

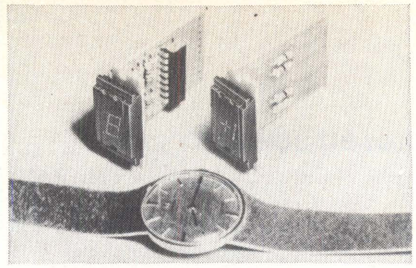


A redesigned LSI version of the company's originate/answer acoustic coupler, which used discrete logic, model 702B offers improved reliability as well as advanced filtering technique. Using a phase-lock loop filtering system, the device is designed particularly to operate where line conditions create data transmission problems. It can be used for terminal-to-terminal or terminal-to-computer operation and features TTY (20-mA current loop) and RS-232 terminal interface, half- or full-duplex switching, and optional hardwire (DAA) connection. **Omnitec Corp,** 2405 S 20th St, Phoenix, AZ 85034.
Circle 229 on Inquiry Card

SERIAL-TO-PARALLEL INTERFACE IC

A single n-channel, Si-gate IC designed to interface serial data communications with parallel digital systems combines functions of two existing IC chips into a single chip. Compatible with IBM BiSync and other modes, UC1671B asynchronous/synchronous transmitter/receiver (ASTRO™) handles full-duplex data rates of up to 1 million baud. It also features transparent mode capability for min system interfacing. 5- to 8-bit word lengths can be selected by either a control word or hardwiring to set up the chip. **Western Digital Corp,** 3128 Red Hill Ave, Newport Beach, CA 92663.
Circle 230 on Inquiry Card

0.27" LED READOUTS



740-0005 is a 0.27", 7-segment, bright red LED char with decoder/driver to produce numbers 0 thrugh 9. -0007 is a plus/minus sign and a 1. Both have decimals and appropriate resistors and are immune to shock and vibration. Decoder/driver requires four lines or bits of information in 8421 BCD code. Terminals on the PC board allow automatic blanking of leading and/or trailing edge zeros, and a lamp test overrides BCD inputs to check for possible display malfunctions. **Dialight, a North American Philips co,** 203 Harrison Pl, Brooklyn, NY 11237.
Circle 231 on Inquiry Card

HIGH SPEED, LOW DRAIN SOS RAM

SCM5520S is a 256-bit CMOS device that is pin compatible with comparable bipolar and n-channel MOS RAMs. Access time is <100 ns; typ values from production measure 50 to 80 ns. Also featured are low power drain and operating power at 1-MHz cycle rate of 5 mW typ. Only 2-V battery backup is needed to store data. Unit is supplied in a 16-pin ceramic package. **Solid State Scientific Inc,** Montgomeryville, PA 18936.
Circle 232 on Inquiry Card

LINE-POWER DISTURBANCE TESTER

To test susceptibility of electronic equipment to power disturbances, the NSG200 simulates short breaks or voltage changes, potentially destructive, superimposed high-energy pulses, and fast interference pulses which may be generated by switches and static discharges. Its modular mainframe accepts individual plug-in units which simulate different types of interference, permitting thorough analysis of circuit behavior to ensure design integrity. **Aikenwood Co, Zi-Tech Div,** 223 Forest Ave, Palo Alto, CA 94301.

Circle 233 on Inquiry Card

COUNTER/CONTROLLER

KE provides high speed up/down counting on a 5-digit LED display with 0.3" high char. Count capacity is expandable by cascading to 10, 15, or more digits. Features include 1-MHz counting rate; battery backup; external programmability; independent preset memory to allow online multilevel control; optional piggyback power supply; TTL, relay, or transistor output; automatic recycling without loss of counts; and power requirement of 5 Vdc ±5% at 2.2 W. **Sodeco/Landis & Gyr,** 4 Westchester Plaza, Elmsford, NY 10523.
Circle 234 on Inquiry Card

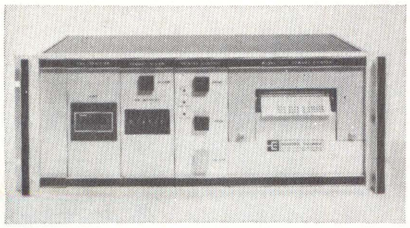
GRAPHICS SYSTEM

Consisting of a vector generator and large screen (up to 21") electrostatic display oscilloscope, QVEC produces XY deflection voltages for the oscilloscope from digital information stored as a display file in the user's minicomputer memory. 10-bit resolution is used for each axis, allowing pictures to be drawn on a 1024 x 1024 grid. Various modes of operation allow dots, absolute and incremental vectors, and alphanumeric char to be drawn at high speed. **Sigma Electronic Systems Ltd,** 37 King Charles Rd, Surbiton, Surrey, England.
Circle 400 on Inquiry Card

ARABIC CHARACTER DISPLAY

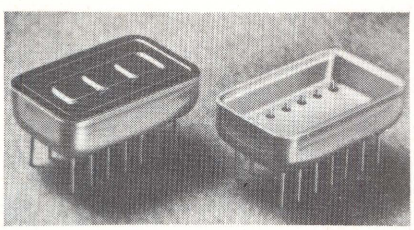
Q620 controller generates 64 Arabic char, including numerals and u/l case, allowing the user to transcribe the language in an 80-char x 24-line display format. Char which must connect may do so. Ascenders and descenders are provided, and a command function places a Nuqta (•) over a char when required. Write operation is from right to left with char entered and displayed on the bottom line of the screen. Display is written from a 5-level CCITT serial data source at 50 baud. **Ann Arbor Terminals, Inc,** 6107 Jackson Rd, Ann Arbor, MI 48103.
Circle 237 on Inquiry Card

DEMAND PRINTER/ALARM



The 9100 is designed to offer a solution to electric power demand monitoring and control. Automatic printout includes day, time to the minute, and kilowatt demand. An optional alarm may be used for manual or semiautomatic control during pk usage periods; an optional KWH meter may be provided for a complete demand/energy study and permanent record. Experimentation by shedding various loads for specific time periods allows the unit to determine effects and feasibility of demand control. **Scientific Columbus,** 1035 W 3rd Ave, Columbus, OH 43212.
Circle 235 on Inquiry Card

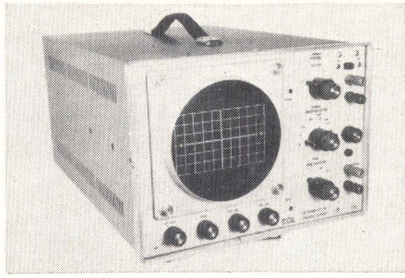
HYBRID MICROELECTRONICS PACKAGE



The Tekform, a single-piece, plug-in Uniwall™ metal microcircuit package, features 0.04" thick walls and base materials made of iron-nickel-cobalt alloy, ASTM Spec F-15. Package cavity and sidewalls are formed as a single unit, eliminating the need for braze joints. Substrate attach area is enclosed by sidewalls, protecting the circuit work surface from damage during assembly. Terminal seals are low thermal expansion-matching borosilicate glass. Fifteen std substrate sizes range from 0.25 x 0.55" to 1 x 1.64", with up to 63 leads. **Tekform Products Co,** 2770 Coronado, Anaheim, CA 92806.
Circle 236 on Inquiry Card

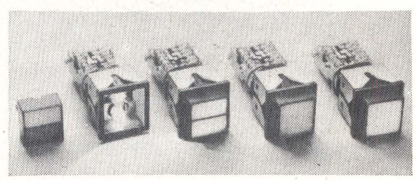
PRODUCTS

SOLID-STATE OSCILLOSCOPES



Model 170 is a dc to 1.5-MHz scope having a 5" flat-faced CRT. Vertical sensitivity is 20 mV/cm, input impedance is 1 MΩ shunted by 30 pF, and sweep frequency is 10 Hz to 100 kHz. Model 170T includes triggered sweep (10 μs/cm). Model 230 has a bandwidth of dc to 5 MHz, sweep frequency of 10 Hz to 500 kHz. Model 230T features sweep speed to 1 μs/cm. **EDL Instruments, Inc,** 6366 Gross Point Rd, Niles, IL 60648.
Circle 238 on Inquiry Card

LIGHTED SNAP-IN PUSHBUTTON SWITCH



300SL series offers up to 4pdt switching capacity and 100,000-cycle max life, no load. Momentary or push-push action as well as single or split legends are available. Lamp terminals are independent of switch terminals, and PC lugs are available for the switch only. Contact resistance is <10 mΩ initially. Electrical ratings are 0.5 A at 28 Vdc, 0.25 A at 110 Vac, 6000 operations under load (silver-plated brass), and 1 A at 28 Vdc, 0.5 A at 110 Vac, 50,000 operations under load (silver alloy). **Oak Industries Inc, Switch Div,** Crystal Lake, IL 60014.
Circle 239 on Inquiry Card

MICROPROCESSOR COMPONENTS

N3001 microprogram control unit and N3002 2-bit central processing element are said to offer 30% faster clock cycle time (45 ns typ) than corresponding devices. In addition, through use of ceramic packages, case temp is significantly lower, providing higher reliability. **Signetics Corp,** 811 E Arques Ave, Sunnyvale, CA 94086.
Circle 240 on Inquiry Card

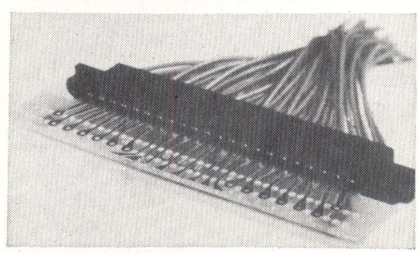
POWER SUPPLY WITH BATTERY BACK-UP

A 5-V, 6-A power supply featuring auxiliary battery back-up, the microcomputer memory power supply automatically maintains permanent power on a 4K x 8-bit memory bank of 2102 RAMs. The standby battery pack is continuously trickle-charged as long as line voltage is present. Power outages from 1 wk to 1 mo long result in no data loss. The open-frame modules are short-circuit proof, and provide overvoltage crowbar protection. **Scarpa Laboratories, Inc,** 46 Liberty St, Brainy Boro Station, Metuchen, NJ 08840.
Circle 241 on Inquiry Card

SWITCHING POWER SUPPLY

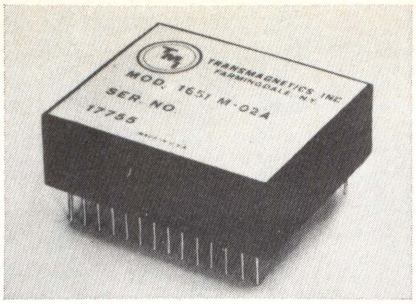
800 series regulated supply provides 1500 W in a package measuring 5.25 x 9.12 x 14.38" and weighing <23 lb. Output voltage is 5 Vdc, 300 A, with 50-mV pk-pk ripple/noise on the output. Line regulation is 0.2%; load, 0.4%; response time is 200 μs; and typ efficiency is 75% for 5-V outputs. Featured are a built-in EMI filter, thermal overload switch, overvoltage protection, remote sensing, and long hold-up time. **LH Research, Inc,** 2052 S Grand Ave, Santa Ana, CA 92705.
Circle 242 on Inquiry Card

DUAL ROW PC BOARD EDGE CONNECTOR



4338 series Edgecon dual row connector, available in eight through 30 dual contact positions, with 0.156" contact spacing, features crimp-type contact and low moisture absorption, dimensionally stable housing. Terminals have a bifurcated contact and are available with pre-tinned plating or gold-over-nickel plating. Anti-overstressed tabs help prevent terminal from collapsing if the PC board is inserted on an acute angle. Wire barriers are also available. **Molex Inc,** 2222 Wellington Ct, Lisle, IL 60532.
Circle 243 on Inquiry Card

TRACKING S-D CONVERTER



Model 1651, a 14-bit tracking synchro-digital converter has 14-bit resolution and 4-min. accuracy. This miniaturized solid-state device continuously transforms synchro or resolver data into digital form that are error free, at tracking rates to 5760 deg/s. Type 2 servo loop error processing techniques insure that data are always fresh and continuously available. Reference and signal inputs are transformer isolated and TTL/DTL compatible. Std inputs are 11.8 or 90 V rms line-to-line, 50 Hz to 10 kHz. **Transmagnetics, Inc,** 210 Adams Blvd, Farmingdale, NY 11735.
Circle 244 on Inquiry Card

MEMORY EXPANSION PACKAGE

In addition to a more extensive instruction set, memory expansion option provides 4 kilobytes of RAM capacity for programming, while TICOL II, an enhanced programming package, expands the types of applications programs that can be implemented on the company's model 742 programmable data terminal. Users may retrieve data from tape cassettes in one-third the amount of time previously required, perform relative addressing of memory, direct transfer of data to and from memory, and receive data from communications lines for direct processing by their program. Programs previously written for the 742 will be fully compatible with models having expanded memory. **Texas Instruments Inc, Digital Systems Div,** PO Box 1444, M/S 784, Houston, TX 77001.
Circle 245 on Inquiry Card

MICROPROCESSOR TEST SYSTEM

A computer-controlled test system which performs high speed functional tests and fault diagnoses on microprocessors and other complex digital logic circuits on PC boards, model 103 of the System 390 series incorporates a 2-family digital word generator/receiver that enables the user to test up to four different levels of logic simultaneously. Bidirectional pins allow testing of bidirectional buses in real time, and enable testing of associated RAMs, ROMs, shift registers, and the CPU. **Instrumentation Engineering, Inc,** 769 Susquehanna Ave, Franklin Lakes, NJ 07417.
Circle 246 on Inquiry Card

SOLID-STATE FREQUENCY CONVERTERS

Offered in 2.5-, 5-, 10-, 15-, 25-, and 30-kVA sizes in single- and 3ϕ, No-Break power system combines battery charger, battery bank, solid-state inverter, and bypass facility to provide disturbance-free, continuous power to critical loads. Charger converts ac mains power to dc. Under normal conditions, dc power float charges the battery and simultaneously provides power for the inverter. Upon serious distortion and/or loss of input ac mains, inverter continues to supply critical load with uninterruptible ac power. **Manufacturing Processes Ltd,** Belvedere Works, Pump Lane Industrial Estate, Hayes, Middlesex, England.
Circle 401 on Inquiry Card

4 x 80-BIT n-CHANNEL SHIFT REGISTER

Featuring a single 5-V power supply, M 142 is an n-channel Si-gate MOS device consisting of four 80-bit registers, each having a control input to enable external data to be shifted into it or output data to be recirculated back into it. Operating frequency range is from dc to 3 MHz. The device is supplied in a 16-lead DIL ceramic and plastic package. **SGS-ATES Semiconductor Corp,** 435 Newtonville Ave, Newtonville, MA 02160.
Circle 247 on Inquiry Card

PRODUCTS

BELL-COMPATIBLE MODEM

The ESP-201, a 201-compatible modem, is suited for mixed system applications since it automatically senses interface requirements and provides the necessary response. When switched to a dial line, it automatically provides fast turnaround (echo suppression protection); when switched to an autodial line, the answer-back tone; or when switched to a Bell modem, necessary handshake interface. Other features include built-in diagnostic testing, data quality indicator, status indicator lamps, manual busy-out switch, and a call-abort timer. **Syntech Corp,** 11810 Parklawn Dr, Rockville, MD 20852.
Circle 248 on Inquiry Card

4K BIPOLAR MEMORY BOARD

Designed for use in systems where high speeds are required, such as complex simulation problems and ultra-fast control response, MS11-AP memory matrix board features 4096 words of bipolar parity memory for PDP-11/45 and /50 computers. Up to 32,744 words can be installed, as opposed to the previous max of 8192. **Digital Equipment Corp,** Maynard, MA 01754.
Circle 249 on Inquiry Card

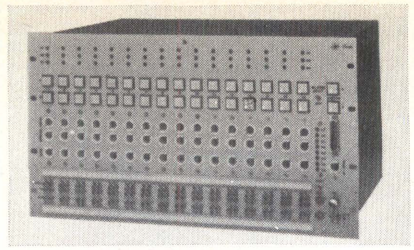
SLIDE SWITCH

MSS-2450 is a 2-pole, 4-position subminiature switch designed specifically for printed circuit applications. Silver-plated brass terminals and beryllium-copper contacts are std. Optional is $1.25\text{-}\mu$ gold plate over nickel. Positive wiping action assures low contact resistance. Four corner tabs add stability when the devices are mounted free-standing on PC boards. **Alco Electronic Products, Inc,** 1551 Osgood St, North Andover, MA 01845.
Circle 250 on Inquiry Card

16- AND 22-PIN 4K RAMs

Employing small die size, single-transistor cell design, and n-channel processing, S4021 devices are pin compatible with TMS4060/2107B and MK 4096. Max access time can be 200, 250, 300, or 400 ns. Low power dissipation results from an avg I_{DD} supply current of 30 mA typ, 40 mA max. Read/write cycle time is 375 ns min, and read/modify/write cycle time is 520 ns min. **American Microsystems, Inc,** 3800 Homestead Rd, Santa Clara, CA 95051.
Circle 251 on Inquiry Card

CONTROL MODULE

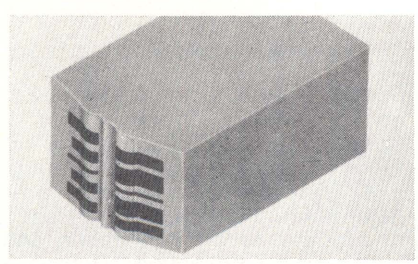


This combined programmable digital fallback switcher with 4-wire VF signal patching permits re-routing signals for 16 channels at both the digital and analog sides of modems. It handles 16 full-duplex RS-232-C digital channels and 16 4-wire VF channels. In the digital interface, unit covers individual channels or all 16 as a group. LEDs provide continuous monitoring of transmit data, receive data, and carrier for each channel. When carrier is lost on any channel, an audible alarm sounds. **Cooke Engineering Co, div of Dynatech Laboratories, Inc,** 900 Slaters Lane, Alexandria, VA 22314.
Circle 252 on Inquiry Card

DAC AND ADC MODULES

CyMOS family features total power requirements of from 100 to 150 mW. Modules can be powered with a 5- to 15-V logic supply applied to a single terminal; voltage used determines logic threshold level. Analog supply voltage may be from ± 10 to ± 15 V. Family includes 8-, 10-, and 12-bit binary units and 2- and 3-digit BCD units. Both complementary binary and straight binary as well as BCD codes are available. **Cycon, Inc,** 1240 Elko Dr, Sunnyvale, CA 94086.
Circle 253 on Inquiry Card

CASSETTE TAPE HEADS



Line of 0.15" format read-after-write digital cassette magnetic tape heads feature guaranteed feedthrough of $<2\%$ at 10 in./s, 150% of saturation, $2\text{-}\mu s$ rise time, and 1600 fci. Available in either one or two channels, and having an all-metal face for long wear, heads meet ANSI, ECMA, and ISO stds. They are offered with a precision base dimension when required, and are designed for high-rel digital cassette transports demanding minimum feedthrough. **Creative Magnetics, Inc,** 49 E Industry Ct, Deer Park, NY 11729.
Circle 254 on Inquiry Card

250-ns 4K n-CHANNEL RAM

The 4096, a 16-pin, 4096-bit n-channel dynamic circuit featuring 250-ns access time, utilizes a single-transistor memory cell and silicon nitride capacitor technology. A 300-ns access time version is also available. Both are housed in a ceramic DIP and are fully TTL compatible. Power dissipation is specified at 250 mW, and typ active access power is 120 mW. Address multiplexing/latching method allows reduction in package size, permitting 80% increase in packing density on memory boards. **Fairchild Camera and Instrument Corp, MOS Products Div,** 464 Ellis St, Mountain View, CA 94042.
Circle 255 on Inquiry Card

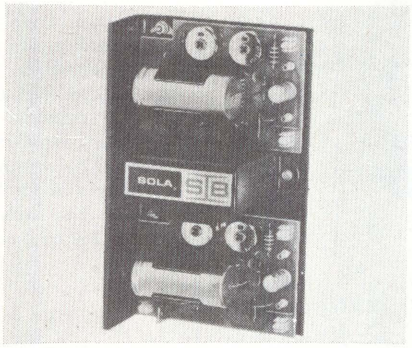
POWER MODULE

Capable of operating over full mil temp range of −55 to 100°C, BN50 series regulate dc input voltages to 0.5% over full input range of 20 to 32 Vdc, converting 28-Vdc input to 50 W of power from 5 to 50 Vdc. Load regulation is 0.5% for no load to full load at constant input voltage. Ripple/noise is 25 mV rms, 100 mV pk-pk, over a range of 25 to 100°C. Other features include full rated output current over −55 to 85°C, derated to 80% of full load rating at 100°C. Tempco is 0.03%/°C. **Abbott Transistor Laboratories, Inc,** 5200 W Jefferson Blvd, Los Angeles, CA 90016.
Circle 256 on Inquiry Card

GAS PLASMA DISPLAY DEVICE

Designed for equipment ranging from POS devices to large scale audience information systems, Self-Scan® II module has 20 char which are 0.7" high and arranged in a 5 x 7 dot matrix alphanumeric display. Orange dots can be seen to 50'; horizontal viewing angle is 150 deg. Only 18 connections are required to control the display. The 14 x 1.9 x <1" panel displays, in addition to ASCII, all Western languages as well as Cyrillic, Hebrew, and Katakana. **Burroughs Corp,** Detroit, MI 48232.
Circle 257 on Inquiry Card

DUAL/TRIPLE-OUTPUT POWER SUPPLIES



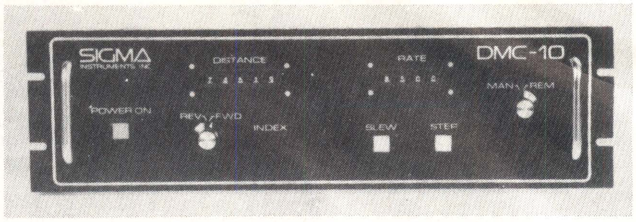
Family of Class 83 series-regulated dc supplies, with dual and triple outputs, features split-bobbin transformer design that provides I/O isolation tested at 1000 MΩ dc, 2500 Vac, and assures full isolation between independent outputs. Each output has individual manual adjustment for both output voltage and current limiting. Reverse voltage protection and short circuit protection with automatic return are built in, and overvoltage protection is available. Input voltages are 120 and 240 Vac, with tolerance for ±10% variation. **Sola Electric,** 1717 Busse Rd, Elk Grove Village, IL 60007.
Circle 258 on Inquiry Card

INDUSTRIAL/MILITARY MODULAR POWER SUPPLIES

Family of militarized line-to-dc encapsulated power supplies is designed to provide high rel performance while operating in rugged environments. MIL-approved, hermetically sealed active components and tantalum capacitors are rated for full operation across specified op temp range. 100% of power is available through 85°C. Storage temp range is −55 to 125°C. Single-output models offer 5 Vdc at 500 and 1000 mA; dual-output versions have ratings of ±12 or ±15 Vdc at ±100 and ±200 mA. **Semiconductor Circuits, Inc,** 306 River St, Haverhill, MA 01830.
Circle 259 on Inquiry Card

PRODUCTS

STEPPING MOTOR CONTROLLER



A programmable controller, the DMC-10 generates and updates speed/distance profiles by means of front-panel thumbwheels or rear-panel remote inputs, and requires no software. Crystal-controlled precision permits max stepping motor speeds without stalling or overshooting target. Jog, Run, and Index functions can be operator-controlled by front-panel buttons or signals brought in from remote inputs (computer or multiplexed BCD inputs) permitting its use for lab testing and debugging of stepping motor systems, or for production line motion control. Inputs are optically isolated from internal logic through special rear-panel terminals to minimize noise and ground loop problems. Output step rate is up to 9990/s; a speed-doubling option is available. **Sigma Instruments, Inc**, 170 Pearl St, Braintree, MA 02184.
Circle 260 on Inquiry Card

DUAL DATA TABLET/DIGITIZER SYSTEM

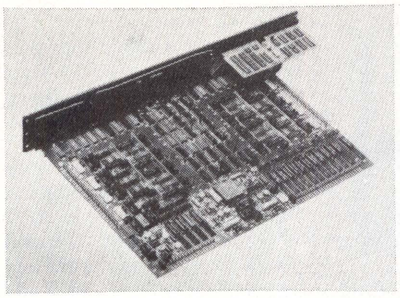
By using a data tablet as a keyboard, the dual system provides economy and flexibility in digtizing graphics and entering alphanumeric, control, and variable data. A 36 x 48" digitizer is used for supplying X-Y coordinate values for applications in cartography, interactive graphics, or CAD; the map, or plan, to be digitized is placed on the surface of the digitizer, and data are entered via either a stylus or cursor. An 11 x 11" tablet, sharing the same controller, is placed on the surface of the large tablet. It usually holds a menu, chart, table, or listing, whose coordinate values have pre-programmed specific meanings, and serves as a "keyboard" to permit entry of both alphanumeric and symbolic data. Basic system offers resolution of 100 or 200 counts/in. **Summagraphics Corp**, 35 Brentwood Ave, Box 781, Fairfield, CT 06430.
Circle 261 on Inquiry Card

DATA LOGGERS

The System 70 series includes six basic Datalogger configurations, each centered around a particular DMM, electrometer, or nanovoltmeter. A 10-channel scanner precedes the measuring instrument in the circuit and an 18-col printer provides a record of time-of-day, channel, data, exponent, and engineering units. The number of input channels can be expanded in multiples of 10. System 70/616/18, an electrometer-based unit, features current sensitivity from 10^{-13} A (0.1 pA) to 100 mA, and is suitable for high impedance ($10^{10}/\Omega$) dc voltage measurements as well. Removable jumpers convert the scanner switching to more conventional voltage configuration of open-circuited idle channels. System 70/160B/18 provides similar results but uses a general-purpose microvolt DMM rather than the electrometer. **Keithley Instruments, Inc**, 28775 Aurora Rd, Cleveland, OH 44139.

Circle 262 on Inquiry Card

ADD-ON CORE MEMORY SYSTEM

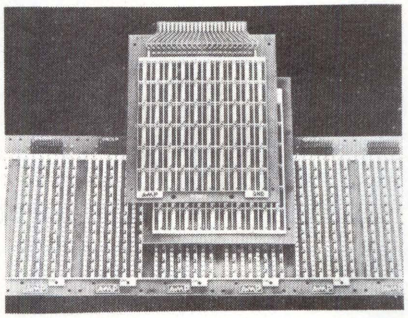


Designed to double the capacity of DEC PDP-11/15 and /20 computers within their available chassis spaces, the 8K-word x 16-bit LM-820 is pin compatible with both. Using a connector block, max storage capacity of 32K words can be achieved by utilizing only four of the available memory card slots within the computer chassis. Two blocks accommodate full internal memory capacity without extra equipment or power sources. Memories have 650-ns cycle time, 280-ns access time, and 86-pin edge-type connectors. **Litton Memory Products, div of Litton Industries,** Canoga Park, CA 91303.

Circle 263 on Inquiry Card

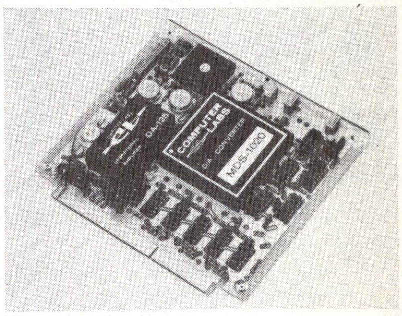
DIP PANELS

Line of DIP and universal IC panels features screw-machined sockets with wrap-type posts and gold-over-nickel plated, seamless beryllium copper contact springs. DIP panels are supplied in 30- or 60-position sizes for either 14- or 16-lead packages; IC panels are provided in 1- to 8-group sizes in the universal 0.1 x 0.3" pattern with each group consisting of nine rows of 50 sockets. All are available with either sockets, posts, or card-edge connector pads for I/O connections. **AMP Inc,** Harrisburg, PA 17105.



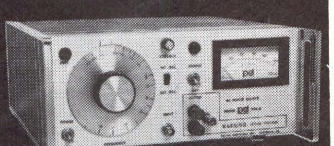
Circle 264 on Inquiry Card

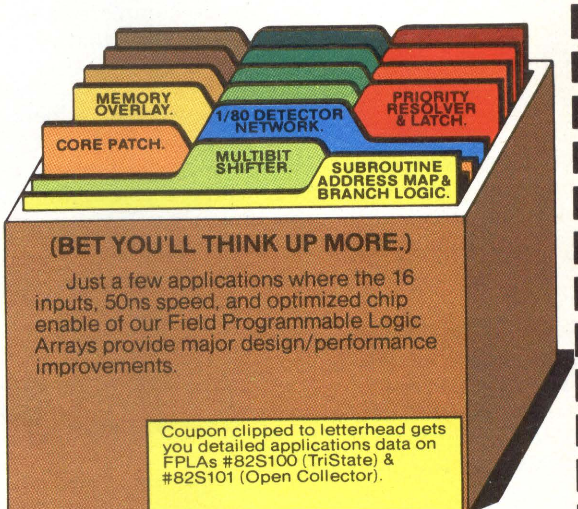
D-A CONVERTERS



TVDA-0815 and -1015 feature an internal deglitcher which suppresses transients in the analog output of the converter, making them useful when reconstructing video signals whose presentation would otherwise be impaired. Std unit provides min settling to either 8- or 10-bit accuracy with slightly over 1 V of output drive into an open circuit; it is suited for applications requiring 1 or 2 V into 50 to 100 Ω. Input word rate for both models is 15 MHz, with accuracies (including linearity) to ±0.05%. **Computer Labs Inc,** 1109 S Chapman St, Greensboro, NC 27403.

Circle 265 on Inquiry Card

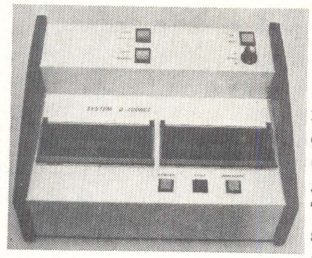




CIRCLE 83 ON INQUIRY CARD

CIRCLE 84 ON INQUIRY CARD

CASSETTE-TO-CASSETTE DUPLICATOR

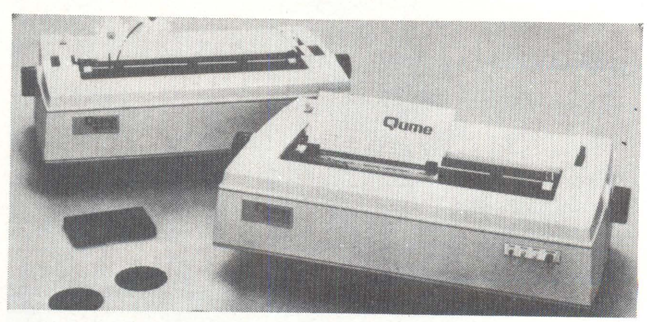


Copying all popular formats of digital cassettes with typ copy time of 30 s for a 100-ft and 90 s for a 300-ft cassette, the D-200 copier meets ISO, ECMA, and ANSI standards for Philips type computer cassettes and is expandable by the addition of slaved copy stations. The unit copies either side A or side B or both tracks at once, and automatically rewinds after making copy. Information can be merged from several cassettes onto one new one to combine program subroutines, data, and text material. Signal and control inputs and outputs are available at a remote receptacle in the rear of the machine. Tape speed is 300 in./s; packing density is up to 1600 fci. **Sunrise Electronics,** 228 N El Molino, Pasadena, CA 91101.
Circle 266 on Inquiry Card

S-D AND D-S CONVERTERS

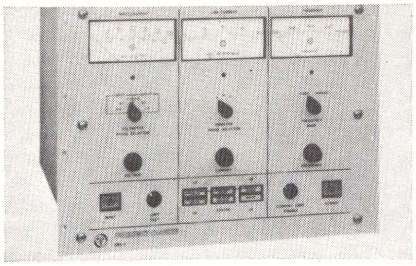
Trigac I converters are available as either PC cards or as cased units, and feature a reference voltage range of 1 to 115 V and a frequency range of dc to 10 kHz, available in any combination; 3-wire, 4-wire, linear dc, or magnesyn inputs; and multiplexing up to 32 channels without system modification. Any number of channels can be multiplexed by addition of a Scott-T or isolation transformer and a FET switch for each channel. Available cards include analog, digital, multiplex, power supply, serial converter, storage register, 28-V buffer, and 400-Hz reference supply. Cased units accept any combination of cards, and include single-channel S-D, 2-channel resolver-to-digital, and 16-channel synchro/resolver-to-digital converters. **The Singer Co, Kearfott Div,** 1150 McBride Ave, Little Falls, NJ 07424.
Circle 267 on Inquiry Card

HIGH SPEED PRINTERS



Sprint 55 and 45 produce letter-perfect final copy at speeds of 55 and 45 char/s, respectively, using the company's daisy printwheel. Both offer a low cost option to increase carbon ribbon life up to 33%; the option is compatible with all existing multistrike carbon ribbon cartridges. The daisy printwheel is positioned by two servomotors for sharp letter registration. Impact on the tall printhammer is automatically adjusted to one of six intensities, to match the size of the character being printed. Critical carriage-to-platen alignment is maintained by a rigid unitized frame and oversized floating guide rails which require no adjustments to maintain straightness. The units print on any form up to 15" wide. **Qume Corp,** 2323 Industrial Pkwy, Hayward, CA 94545.
Circle 268 on Inquiry Card

POWER FREQUENCY CHANGER

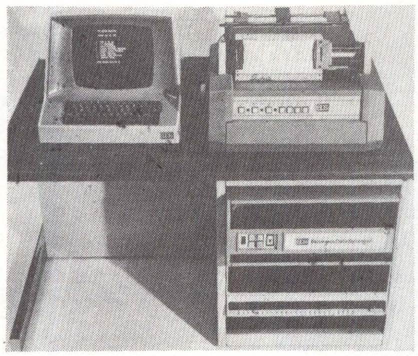


Designed to provide conversion from domestic to foreign or foreign to domestic power line stds for any application requiring a voltage and frequency stable power source such as tape or disc drives, SMG-5-5 operates at 92% nom efficiency, no load idling loss of 2% of ratings, and produces 62-dB sound level. It offers protection from overloads and short circuits, low output impedance, and fast response. Any number of units may be paralleled to increase capacity or obtain redundancy, and a UPS option is available. **A•L•S Electronics Corp,** 733 E Edna Pl, Covina, CA 91723.

Circle 269 on Inquiry Card

SMALL COMPUTER SYSTEM

0/100 consists of a 16K-word CPU, 12 megabytes of fixed disc, a 24 x 80-char CRT, and a 100-line/min. printer. A wide variety of options allows the unit to be tailored for individual end-user requirements. The system utilizes a powerful disc operating system called BDSOS and features EXBASIC, an extended BASIC that supports up to eight users. **Business Data Systems of California, Inc,** 260 Sheridan Ave, Suite 100, Palo Alto, CA 94306.



Circle 270 on Inquiry Card

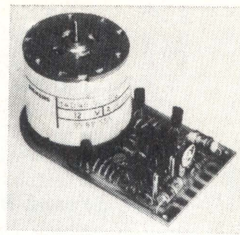
DIGITAL TRANSMISSION MULTIMETER

Model 430 is used to test noise, level, and frequency, as well as line resistance and capacitance, loop current, station battery, and ac power influence of telephone lines. All measurements are made from one input connection, with pushbutton control and digital display of measurement. Signal level (−70 to 15 dBm, 50-kHz bandwidth) and noise metallic (80 to 0 dBrn) are measured with selectable termination impedances and bridging. Built-in C-message, 3-kHz flat and 15-kHz flat filter weighting are provided. **Wavetek, Telecommunication Products,** PO Box 651, San Deigo, CA 92112.

Circle 271 on Inquiry Card

PRODUCTS

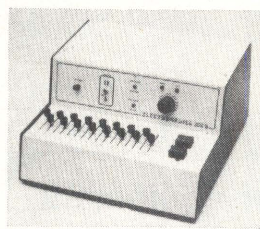
BRUSHLESS DC MOTORS



A field-tested brushless dc motor package, 1AD4002-OQQ99-AF includes the basic motor integral with electronics, designed to run continuously and without service for a min of 10,000 hr, with continuous torque capability of 0.35 oz-in., and a speed adjustment range of 2200 to 3300 rpm. Speed regulation over the entire torque range is 1%. The housing measures 1.57" dia x 1.49" long, and requires a 2-wire input for operation from a 12-Vdc ±5% power supply. The basic motor without electronics has a permanent dynamically balanced alnico IV cylindrical magnet, four windings, and two Hall generators. With an appropriately designed commutator, it has torque capability of 1.2 oz-in., continuously running in the −10 to 55°C temp range. **Siemens Corp, Power Engineering Div,** 186 Wood Ave S, Iselin, NJ 08830.

Circle 272 on Inquiry Card

DIGITAL IC TESTER

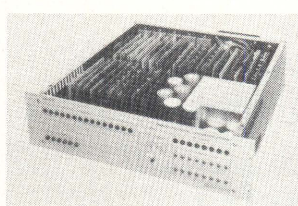


Self-programmable via a switch panel which allows selection of the function for each pin of the device to be tested, the model 1550 provides a separate socket for a known-good reference device. Each pin on the reference and UUT test sockets are wired to receivers which compare the status of corresponding inputs or outputs at each program step. Parallel operation allows ½-s test time for all devices. Data applied to inputs are gray-code weighted and then randomized by enciphering circuits to ensure full functional exercising of the device under test. The machine tests DTL, TTL, CMOS, HTL, and HINIL. Other features include a fault locator switch to identify failed pins, 5-/12-V power supply operation, and handler interface. **Electromedics,** 3295 Brookdale Dr, Santa Clara, CA 95051.

Circle 273 on Inquiry Card

PRECISION A-D CONVERSION SYSTEM

GMAD-4 combines front-panel manual controls with rear-panel interface signals and controls that easily interface with widely used minicomputers and controllers. Available with either 10-, 12-, or 15-bit resolution, the unit interfaces with hardware and software configurations of the DEC PDP-11, HP 2100, Varian V-73, Data General Nova, and other similar computers. Completely enclosed within a 5½" high rack-mounted enclosure are A-D converter, internal clock and addressing circuits, central power supply, and up to 256 single-ended or 128 differential input multiplexer channels. Nom full-scale analog input voltage range is ±10 or ±5 V. Input impedance for the analog input signals is 1000 MΩ, and linearity of the system is within ±0.01%. **Preston Scientific, Inc,** 805 E Cerritos Ave, Anaheim, CA 92805.

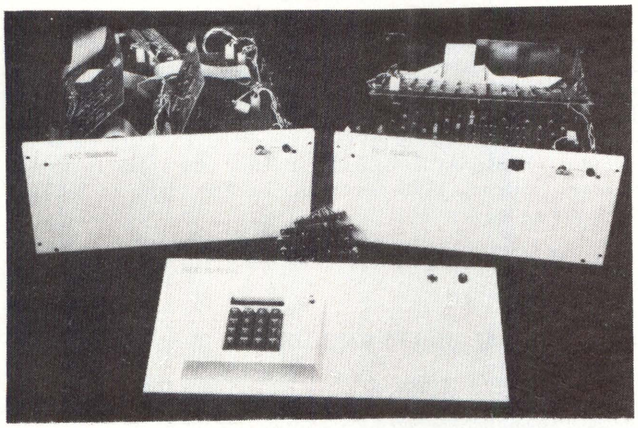


Circle 274 on Inquiry Card

MODULAR POWER SUPPLIES

Offering direct PCB mounting and delivering 10 W of dc output power, model PM597 supplies ±12 Vdc at 400 mA; PM545, 5 Vdc at 2000 mA. The supplies measure 2.5 x 3.5 x 1.62", and are available in popular pin configurations. Specs include: 115 ±10-Vac or 230 ±20-Vac input voltage; 50- to 400-Hz input frequency; and ±400- or 2000-mA output current. Line regulation is ±0.02% max, load regulation is ±0.02% max, and ripple and noise are 0.5 or 1 mV rms. Tempco is 0.02%/°C. **Computer Products, Inc,** 1400 NW 70th St, Fort Lauderdale, FL 33307.
Circle 275 on Inquiry Card

FLOPPY DISC TEST SYSTEM



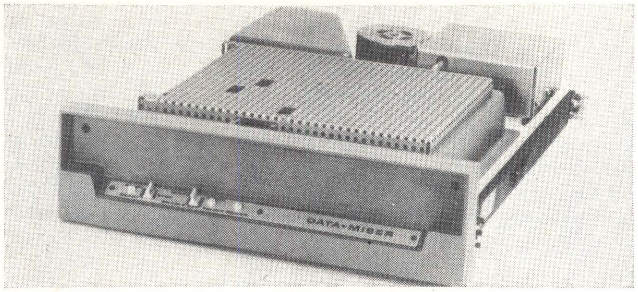
Based on the series 70 microcomputer and series 61 IBM-compatible floppy disc system, test system performs complete diagnostic testing and exercising including error rate, compatibility, and media testing on IBM-compatible floppy disc drives. Various tests and combinations of tests are provided for appropriate use in production assembly testing, receiving inspection testing, QA analysis, and life testing. Test program is supplied on an IBM-compatible floppy disc for initial automatic system load. The test operator specifies tests and test sequence from a CRT or TTY terminal. Thorough test of a disc drive requires 5 min; comprehensive drive and media test and error rate require 15 min. Configurations are available to test 1, 2, 4, 6, or 8 drives. **Applied Data Communications,** 1509 E McFadden Ave, Santa Ana, CA 92705.
Circle 276 on Inquiry Card

PROGRAMMABLE DATA ACQUISITION/TELEMETRY CONTROL SYSTEM

For use on std dial telephone network; radio link, leased line, or private WATS network; or hardwired for in-plant use, model DAS-16C is a 4K-word, processor-based integrated digital system. Compatible with existing process sensors, meteorological sensors, and other analytical instruments, the system interfaces with existing computer peripherals and data acquisition systems. Basic system consists of a central station processor, CRT and/or teleprinter, and a remote data terminal capable of up to 24 analog inputs, 36 status inputs, and 15 remotely controlled output relays. The number of additional remote terminals is limited only by availability of common carrier telephone network or private communications system. **FX Systems,** PO Box 818, 77 Cornell St, Kingston, NY 12401.
Circle 277 on Inquiry Card

PRODUCTS

200-TRACK/IN. MOVING-HEAD DISC DRIVE



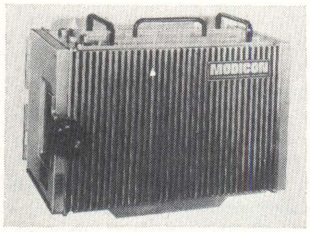
Data Miser™ model DM06 has 5-megabyte capacity, is completely plug-compatible with DEC RK11 and all std DEC operating systems, such as DOS, RSTS, RSX, and RT11, and requires no software modification. In combination with the DM1000 controller, it is completely compatible with the UNIBUS cable as a PDP-11 system expansion. The drive uses a single 14" disc as media. Its head-positioning motor provides 15-ms track-to-track access time, with 120-ms full stroke time and 75-ms average time. Recording density is 2200 bits/in. with a data transfer rate of 1.58 MHz at a disc rotation speed of 1500 rpm. The complete electronic interface is contained on one 10 x 10" PC board. **International Memory Systems,** 14609 Scottsdale Rd, Scottsdale, AZ 85260.
Circle 278 on Inquiry Card

INCREMENTAL SHAFT ENCODER

Offering full-swing square wave output signals capable of 0.1-A sinking capacity for high noise immunity, std OPTACH incremental encoders operate from a single positive supply of 5, 6, or 10 to 15 V with a regulation tolerance of ±20%. Differential configuration of photocells and use of high quality differential amplifiers allow the units to operate at speeds from 100,000 to 500,000 counts/s. Rise or fall times are 0.5 μs max. The units are available in basic, heavy duty, and hazardous duty enclosures. Use of wide-aperture moire optics yields a strong signal which is averaged out over a large number of lines, minimizing effects of pattern imperfections. Differencing the outputs of diametrically opposed photocells results in a balanced symmetrical signal. **HH Controls Co, Inc,** 16 Frost St, Arlington, MA 02174.
Circle 279 on Inquiry Card

PROGRAMMABLE CONTROLLER

A high speed, relay-logic programmed controller, the 384 achieves high speed capability with max utilization of core memory at min logic solving times, for use in applications involving extensive use of data transfer functions. The PC has a 4K read/write core memory, provides three times the logic line capacity of the company's current 4K PC, and contains all data transfer functions now available and can accept future functions. It performs complex data transfer functions such as matrix handling, coupled with multiplication and division, ten times faster than the current machine, yet is hardware compatible and uses the same relay logic symbols, function codes, and references for programming. **Modicon Corp,** PO Box 83, Shawsheen Village, Andover, MA 01810.



Circle 280 on Inquiry Card

LITERATURE

Process Control Computer

Covering the 2570, which contains a 2500 computer and process I/O subsystems, brochure details std I/O hardware, termination options, and std software. **Westinghouse Electric Corp, Computer and Instrumentation Div,** Pittsburgh, Pa.
Circle 300 on Inquiry Card

Data Storage Buffer

Highlighting features of the Comstore 1032, brochure provides application diagrams and specs on the data communications tool. **International Communications Corp,** Miami, Fla.
Circle 301 on Inquiry Card

Uninterruptible Power Systems

Discussing different techniques used to protect both large and small computers, brochure describes both single and redundant UPS configurations. **International Power Machines Corp,** Mesquite, Tex.
Circle 302 on Inquiry Card

Synchro Converters

Brochure contains application and specification information for solid-state synchro converters, describing both digital and analog types. **Natel Engineering Co, Inc,** Canoga Park, Calif.
Circle 303 on Inquiry Card

Computer Products

Photos and descriptions of peripherals and minicomputer operating systems, I/O extenders, and communications interfaces are contained in catalog. **Hewlett-Packard Co, Data Systems Div,** Palo Alto, Calif.
Circle 304 on Inquiry Card

Function/Pulse Generators

Catalog contains data on series 30, 50A, and 70 function generators and pulse generators, and includes an applications selector wheel. **Interstate Electronics Corp,** Anaheim, Calif.
Circle 305 on Inquiry Card

Pushbutton Switches

C160/C170 series snap-action switches are presented in bulletin describing features, electrical and mechanical characteristics, and providing dimensional photos. **Control Switch, a Cutler-Hammer Co,** Folcroft, Pa.
Circle 306 on Inquiry Card

International System of Units

To help in preparing documents using the International System of Units (SI) according to the Federal Information Processing Standards Program, pamphlet is available for 25¢ from the **National Bureau of Standards, Dept of Commerce,** Washington, DC 20234.
Circle 307 on Inquiry Card

Magnetic Tape Units

Catalog illustrates and describes line of tape units, formatters, and controllers, providing specs for 9-track incremental transport, synchronous/asynchronous recorder, and vacuum-column unit. **Kennedy Co,** Altadena, Calif.
Circle 308 on Inquiry Card

Magnetic Disc Memories

Features and specs on the SYS-10 and -20, head-per-track memories designed for use with Nova and PDP-11 minicomputers, are provided in brochures which discuss hardware/software compatibility. **General Instrument Corp, Rotating Memory Products,** Hawthorne, Calif.
Circle 309 on Inquiry Card

Measurement and Control Equipment

Describing design concepts, brochure contains typ configurations for both local and remote applications of the RTP family of computer-independent direct analog and digital I/O equipment. **Computer Products,** Fort Lauderdale, Fla.
Circle 310 on Inquiry Card

Flexible Etched-Circuit Cable Systems

Including descriptions of advantages and manufacturing techniques, brochure contains an application information form listing optional specs for materials, electrical requirements, mechanical, and physical data. **ITT/Cannon Electric Div,** Santa Ana, Calif.
Circle 311 on Inquiry Card

Optoelectronic Devices

252-page *Optoelectronics D.A.T.A. Book* contains electrical, optical, and physical characteristics for more than 5000 devices and assemblies, organized into five major categories: emitters, photocouplers, displays, sensors, and special detectors. Price for a 1-yr, 2-edition subscription is $54.50 in the U.S. ($56.20 elsewhere). **D.A.T.A., Inc,** 32 Lincoln Ave, Orange, NJ 07050.

Dynamic Disc Testing

Brochure details a system for testing assembled single- and double-density computer disc packs at speeds to 3600 rpm under true operating conditions. **ADE Corp,** Watertown, Mass.
Circle 312 on Inquiry Card

Basic UPS Systems

Text, diagrams, and oscillograms in brochure describe continuous, static switching bypass, extended time protection, and parallel-redundant types of UPS systems. **Cyberex, Inc,** Mentor, Ohio.
Circle 313 on Inquiry Card

Flatbed Graphic Plotter

Bulletin pictures the 430/101 Dataplotter[R] and provides technical data, specs, applications, features, and other pertinent information on the high speed plotter. **Broomall Industries, Inc,** Broomall, Pa.
Circle 314 on Inquiry Card

Microcomputer System

Featuring M- (8080-based) and L- (8008-based) series microcomputer system modules, catalog also details development systems, support hardware, software library, and custom design services. **Control Logic, Inc,** Natick, Mass.
Circle 315 on Inquiry Card

Benchtop Power Supplies

Illustrating the unit's stackability, brochure includes electronic and mechanical specs on 11-model line of single-, dual-, and triple-output supplies. **Acopian Corp,** Easton, Pa.
Circle 316 on Inquiry Card

Thumbwheel Switches

Front- and rear-mount versions are described with mechanical and electrical specs as well as data on PC board codes and accessories in catalog that includes easy reference tables. **Inter-Market, Inc,** Glenview, Ill.
Circle 317 on Inquiry Card

Open-Frame Power Supplies

Literature lists Q-series models, specs, and features, and cross-references models by voltage. **Deltron, Inc,** North Wales, Pa.
Circle 318 on Inquiry Card

Wire and Cable

Product guide acts as quick reference for information, listing product insulation, temp rating, AWG range, and approval agencies in easy-to-read form. **Berk-Tek, Inc,** Reading, Pa.
Circle 319 on Inquiry Card

LITERATURE

Dynamic Memory Burn-In Systems

Systems 15 and 12, designed for burn-in of MOS or bipolar semiconductor memory or logic devices, are featured in brochure, which contains a color-coded schematic block diagram showing design organization and function of the systems. **Marin Controls Co, div of FRL, Inc,** Belmont, Calif.
Circle 320 on Inquiry Card

Subminiature Lamps

Specs and drawings of 177 lamps, tips on selecting the proper type, and data on wedge-base and halogen cycle lamps are contained in revised catalog. **General Electric Co, Miniature Lamp Products Dept,** Cleveland, Ohio.
Circle 321 on Inquiry Card

Paper-Tape Reader

Describing working components of the "Fly Reader 30," which requires a single 5-V, 2-A power source, brochure also gives specs, timing diagram, interface connector wiring, and installation drawings. **Teleterminal Corp,** Burlington, Mass.
Circle 322 on Inquiry Card

Intelligent Remote Batch Terminals

Benefits offered by Series 500 terminals are defined in literature that describes the system, customer support program, installation and maintenance procedures, and software and available options. **Singer-M & M Computer Industries, Inc,** Orange, Calif.
Circle 323 on Inquiry Card

Programmed Batching Control

Model 5120, engineered to control a wide variety of batching and blending processes, is described in brochure with details on system operation, features, and components. **StreeterAmet, div of Mangood Corp,** Grayslake, Ill.
Circle 324 on Inquiry Card

Dc Power Supplies

Providing electrical and mechanical specs on 275 std products, selection and reference guide lists key parameters of line-operated, dc-operated, and high-efficiency line-operated supplies, as well as dc-dc converters. **Semiconductor Circuits, Inc,** Haverhill, Mass.
Circle 325 on Inquiry Card

GUIDE TO PRODUCT INFORMATION

NOTE: The number associated with each item in this guide indicates the **page** on which the item appears—**not** the reader service number. Please do **not** circle the page number on the reader service card.

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